

PG142-B00

DP + DP + DP + HDMI/DP

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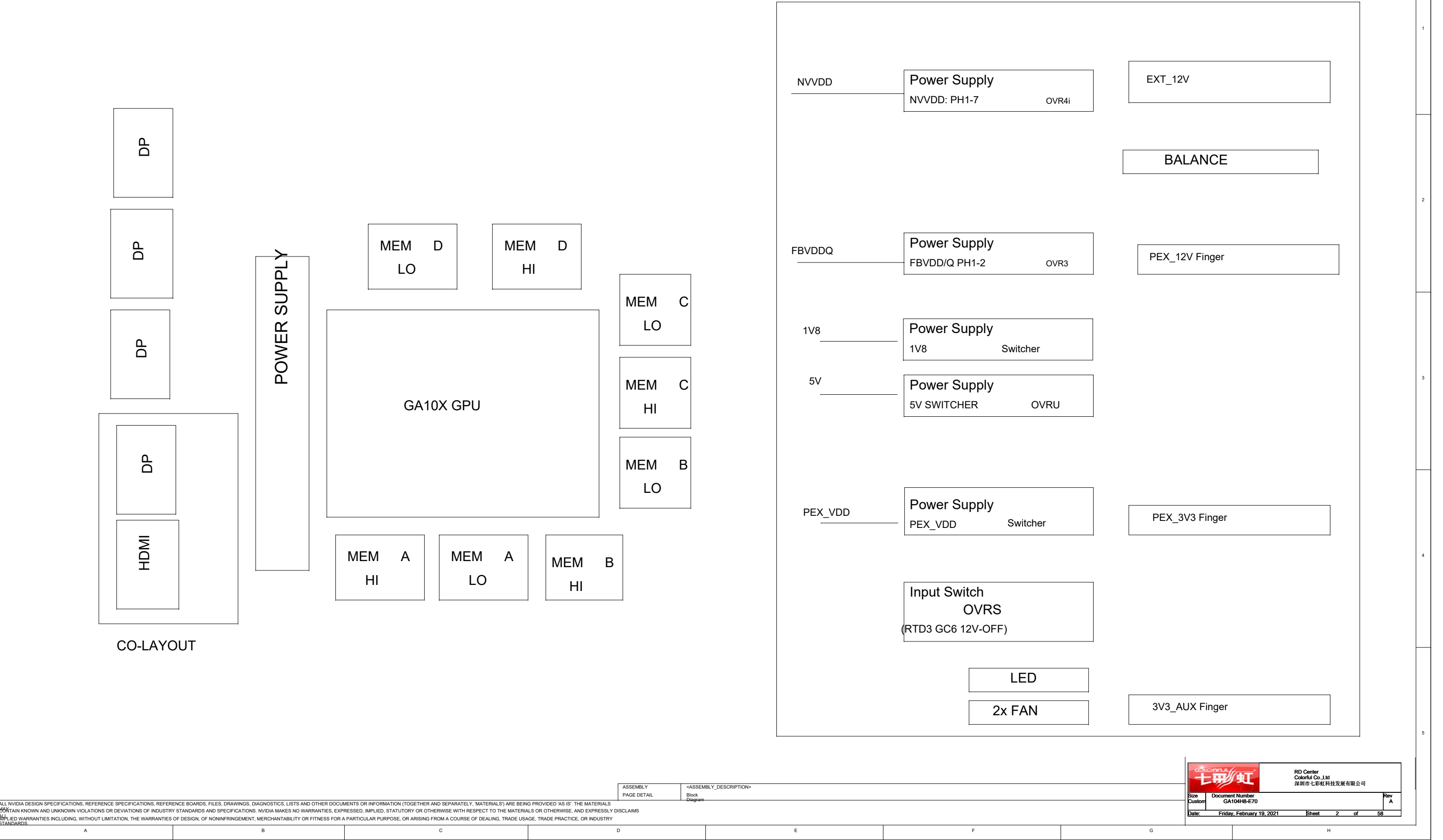
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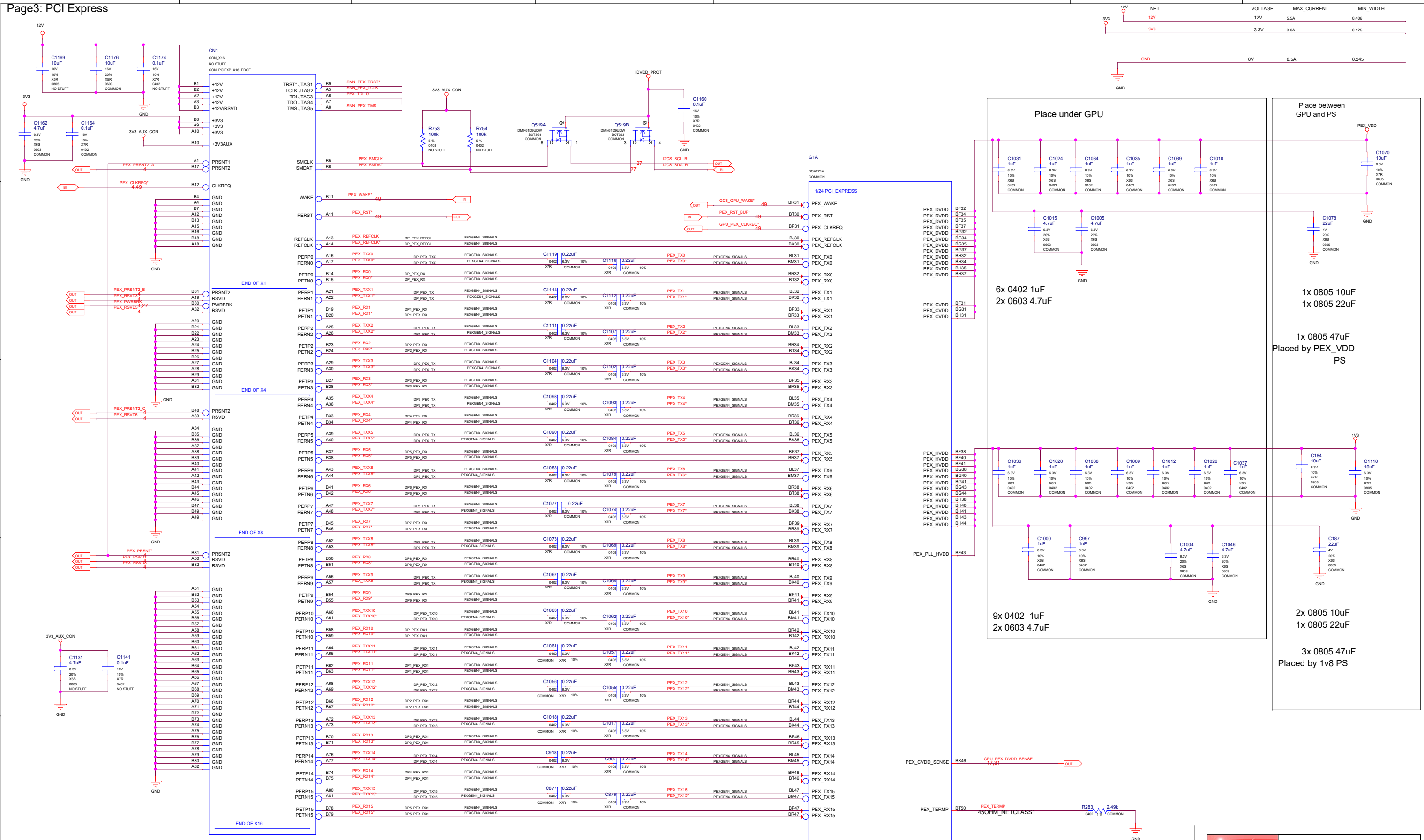
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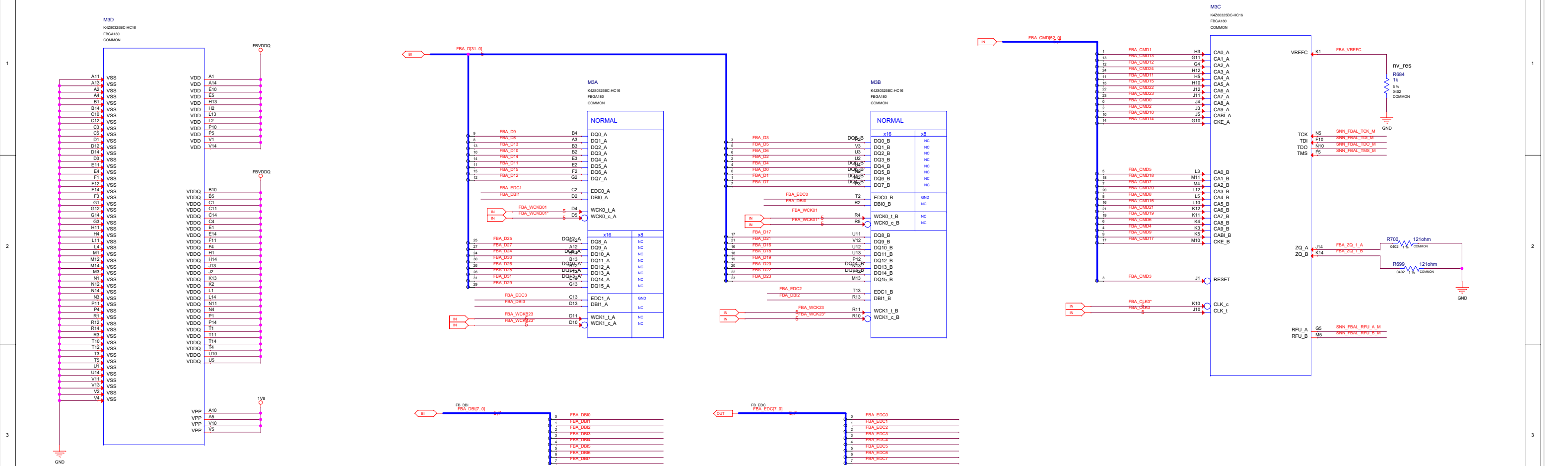
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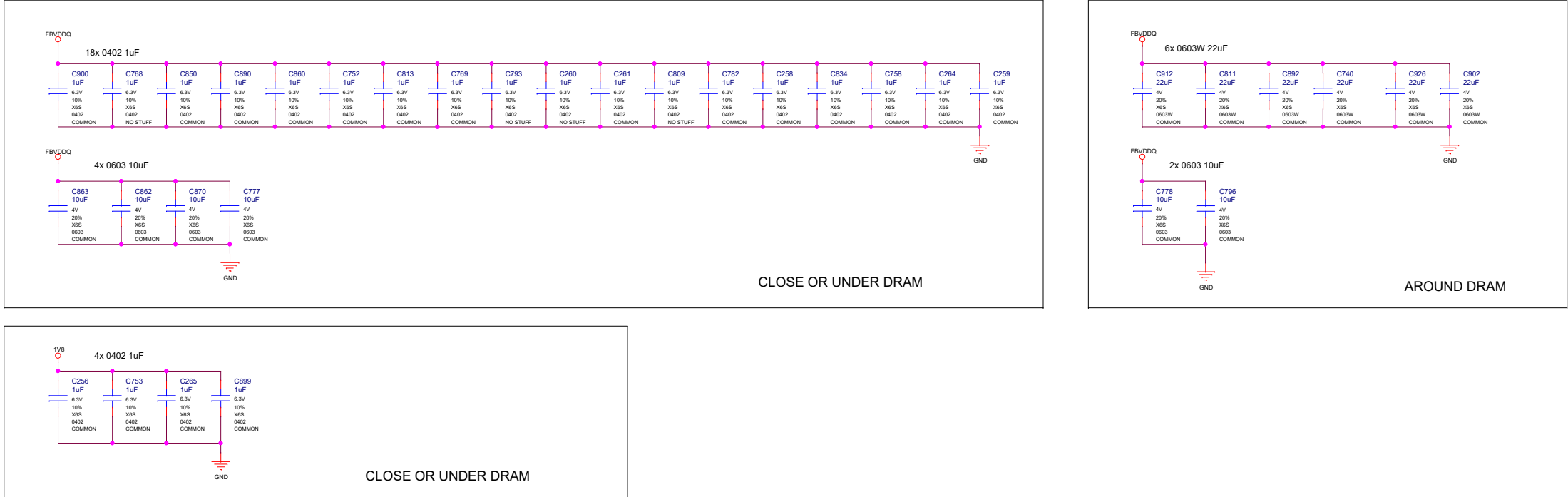
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decap via : at least 2 gnd vias and 2 power vias for each cap




CLOSE OR UNDER DRAM

AROUND DRAM

CLOSE OR UNDER DRAM

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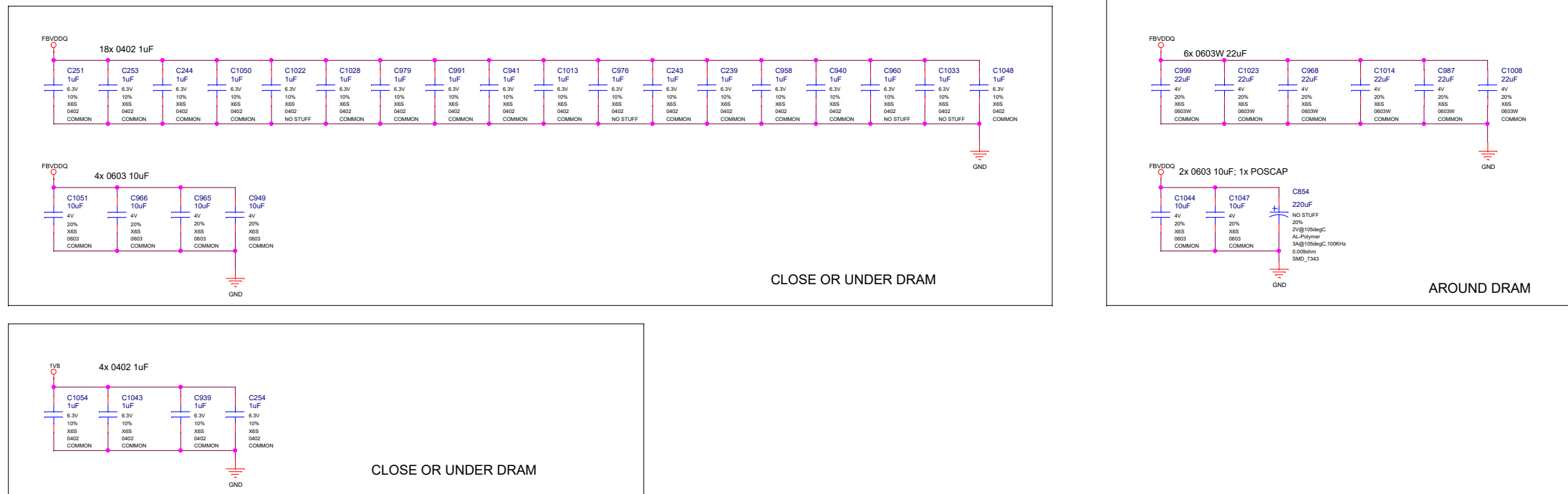
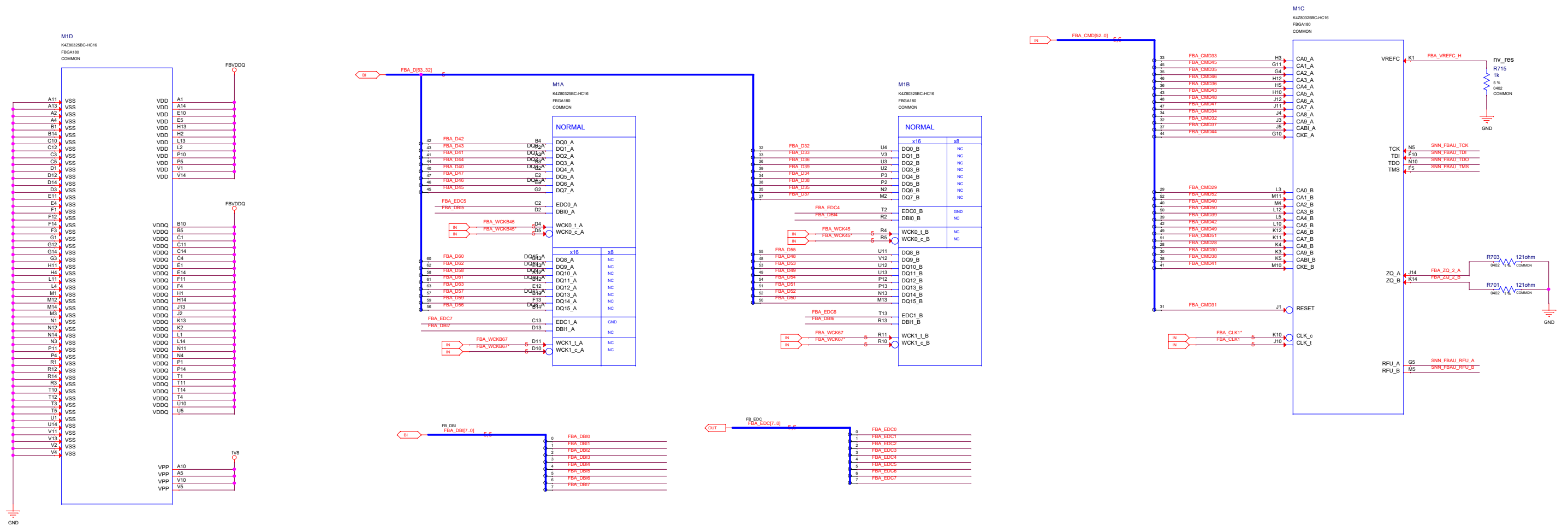
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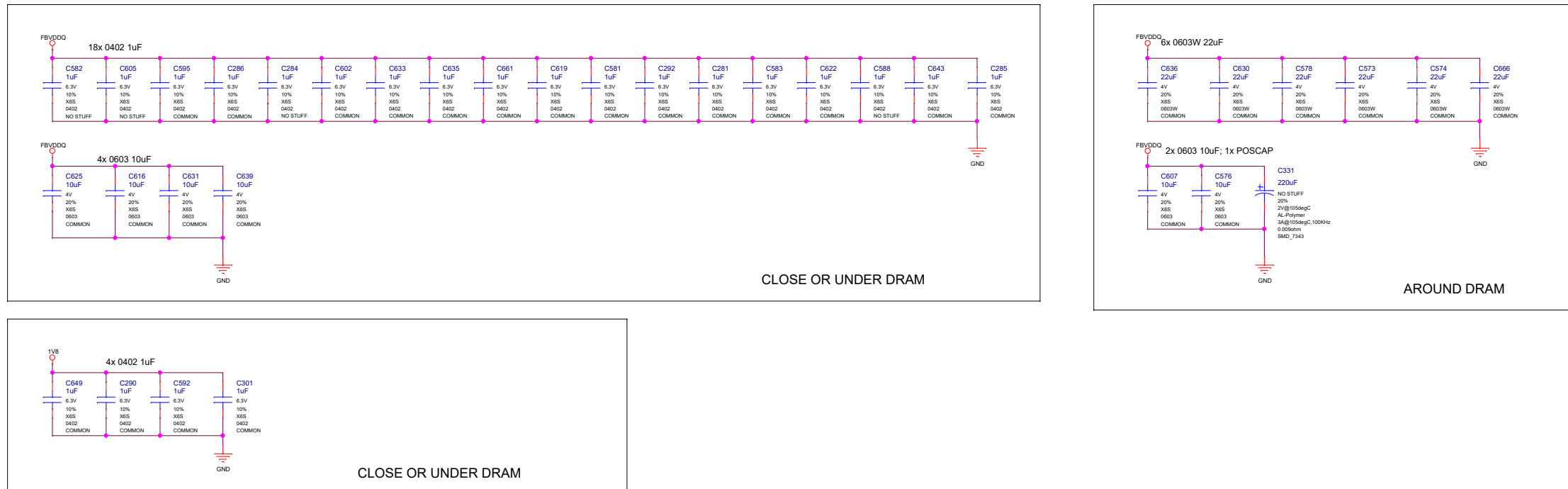
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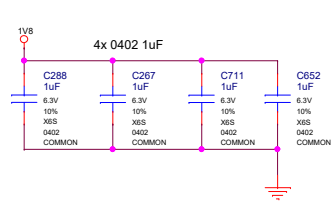
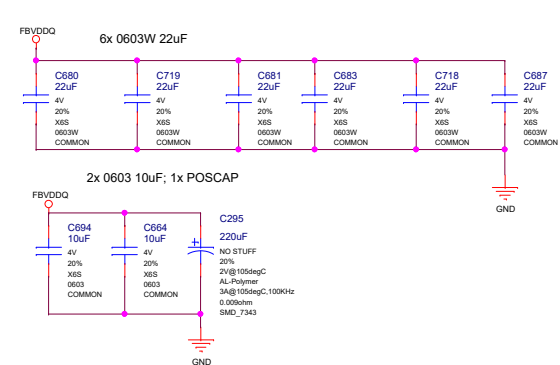
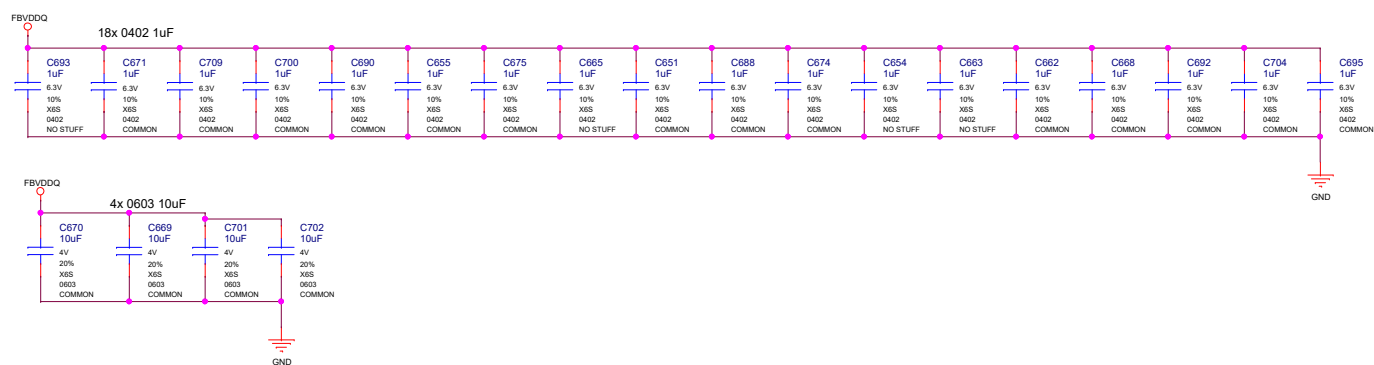
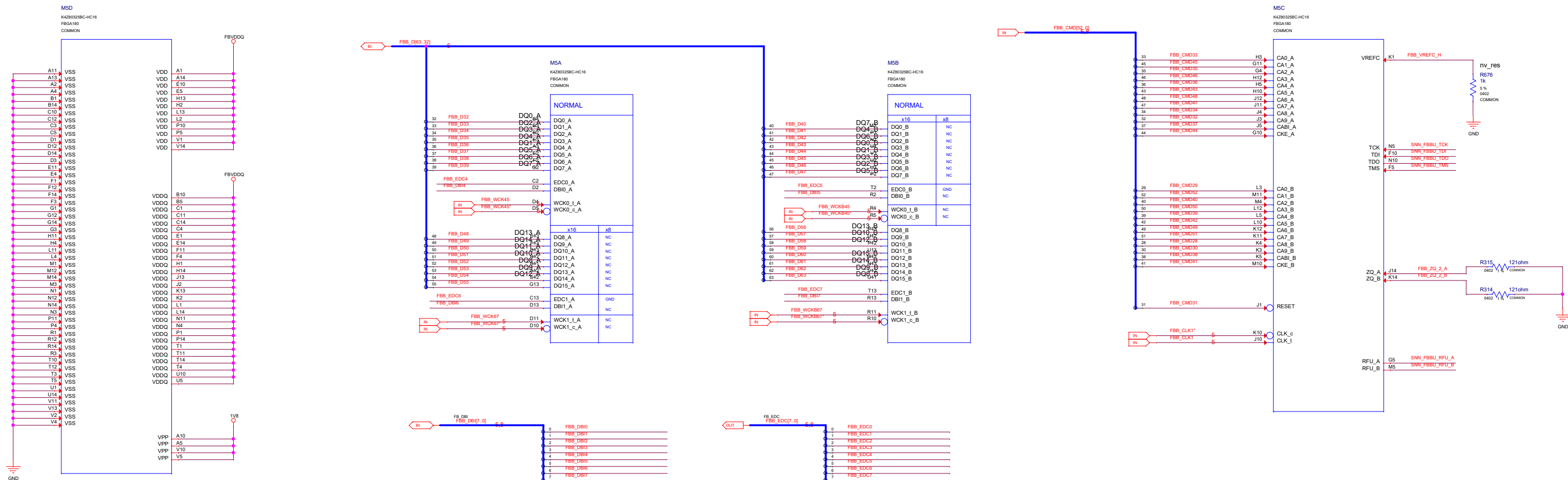


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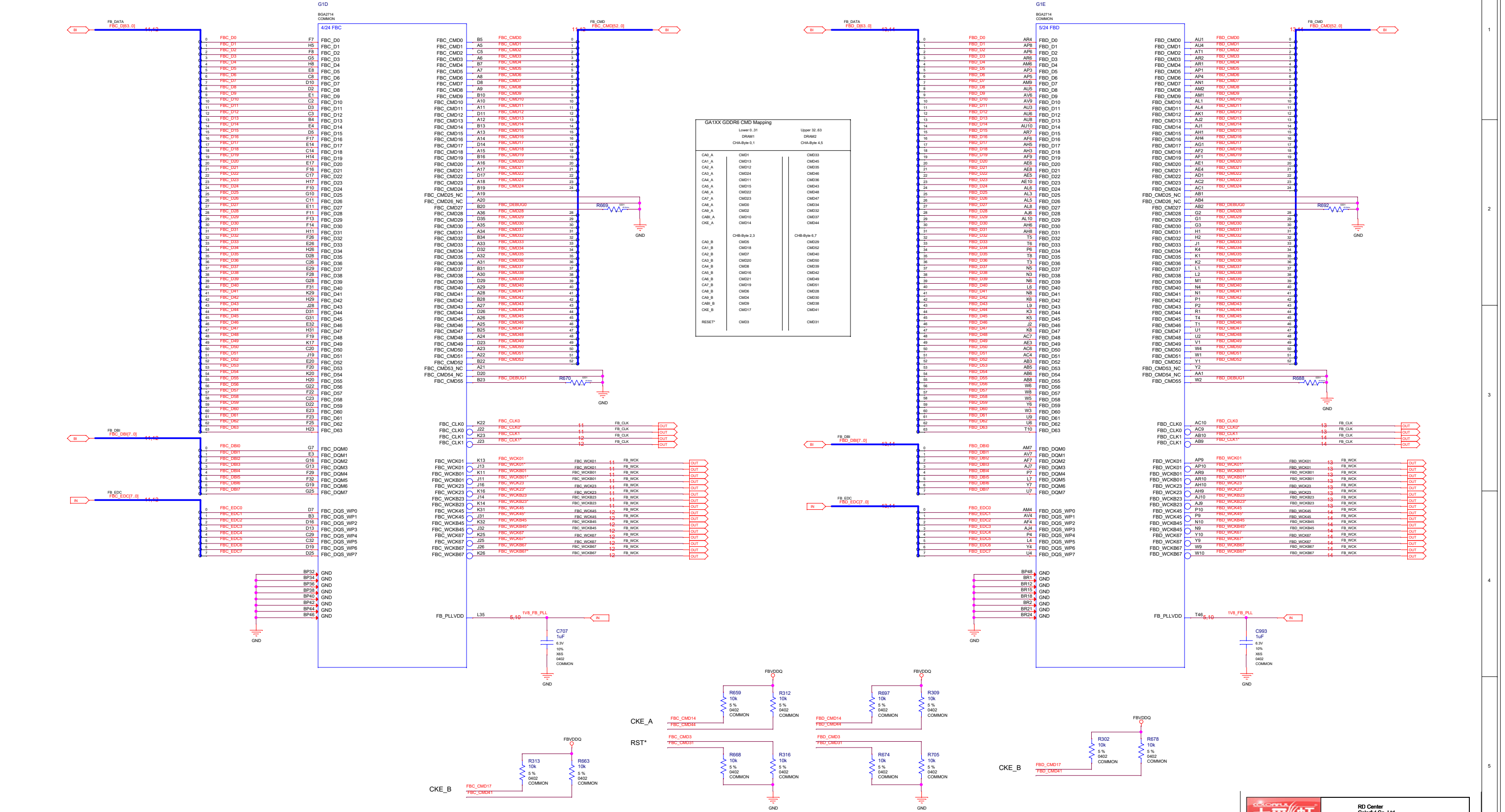
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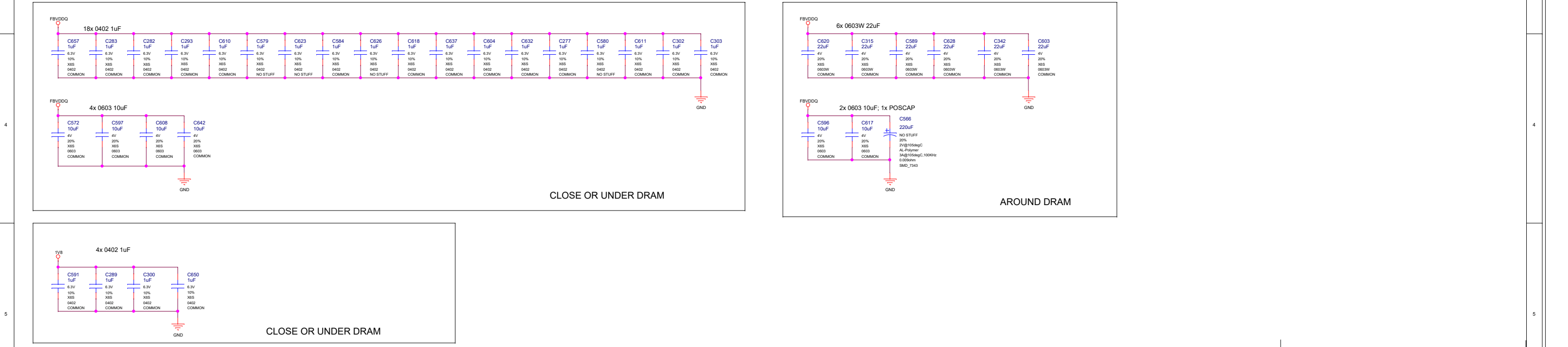
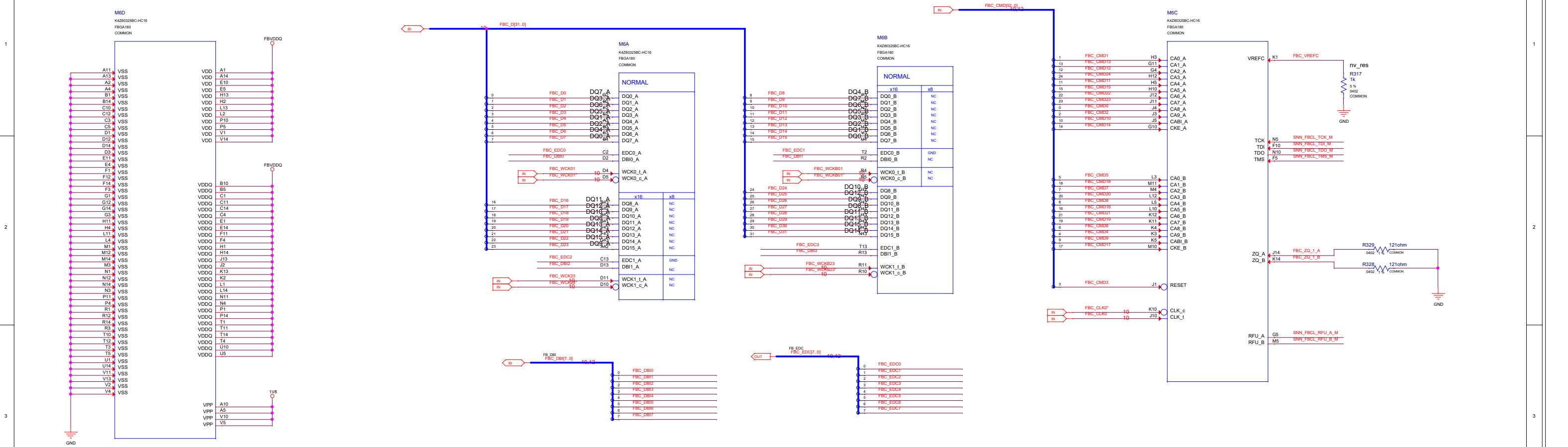
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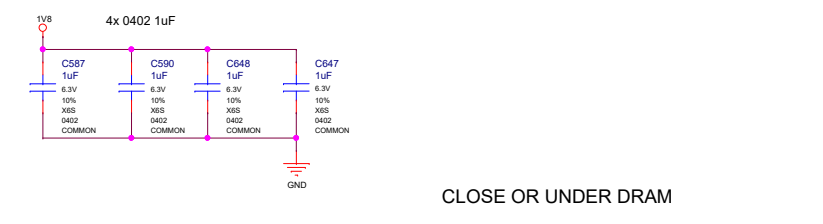
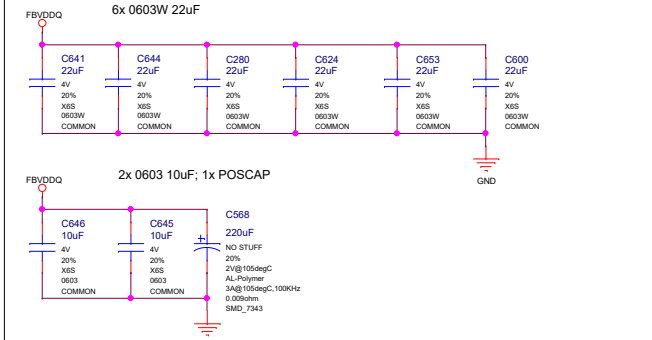
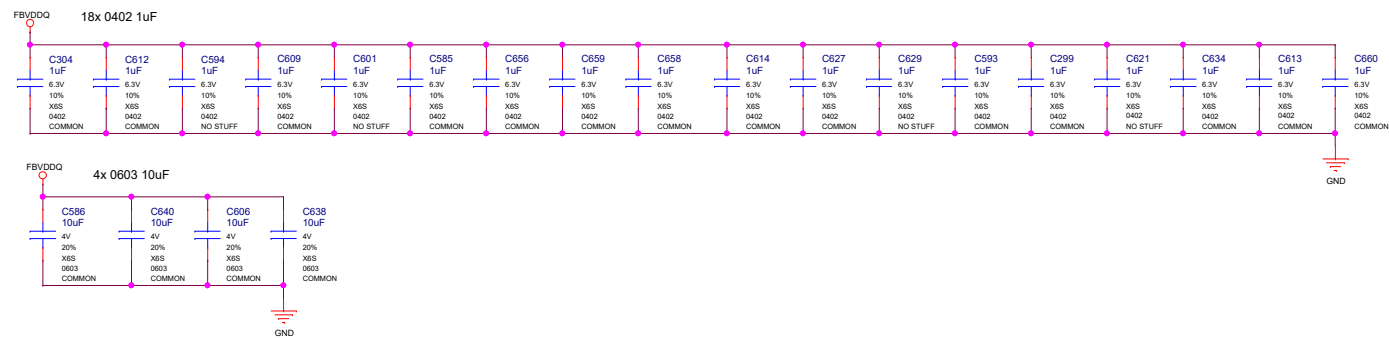
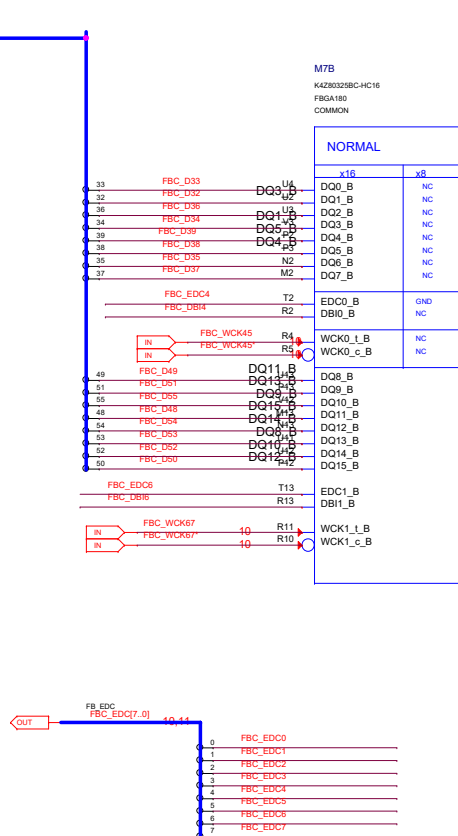
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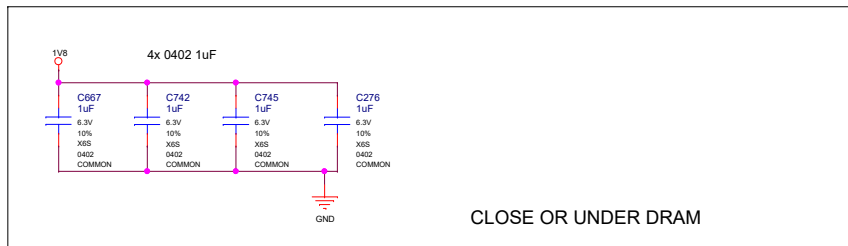
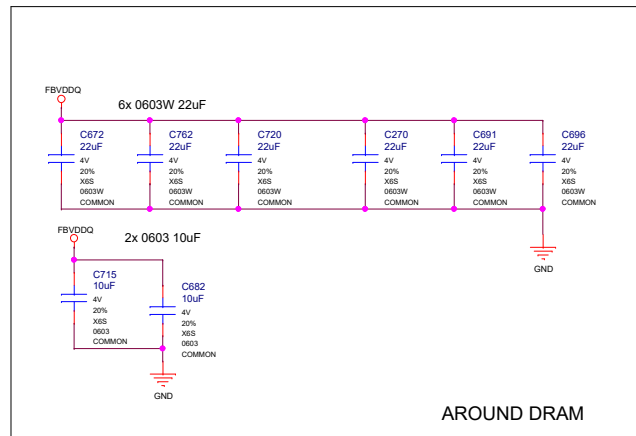
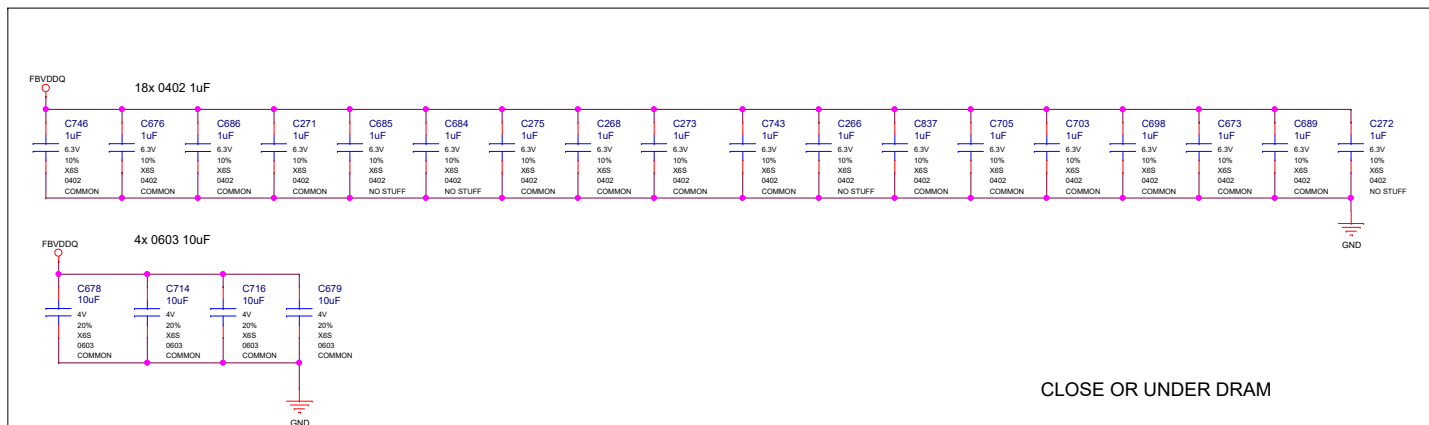
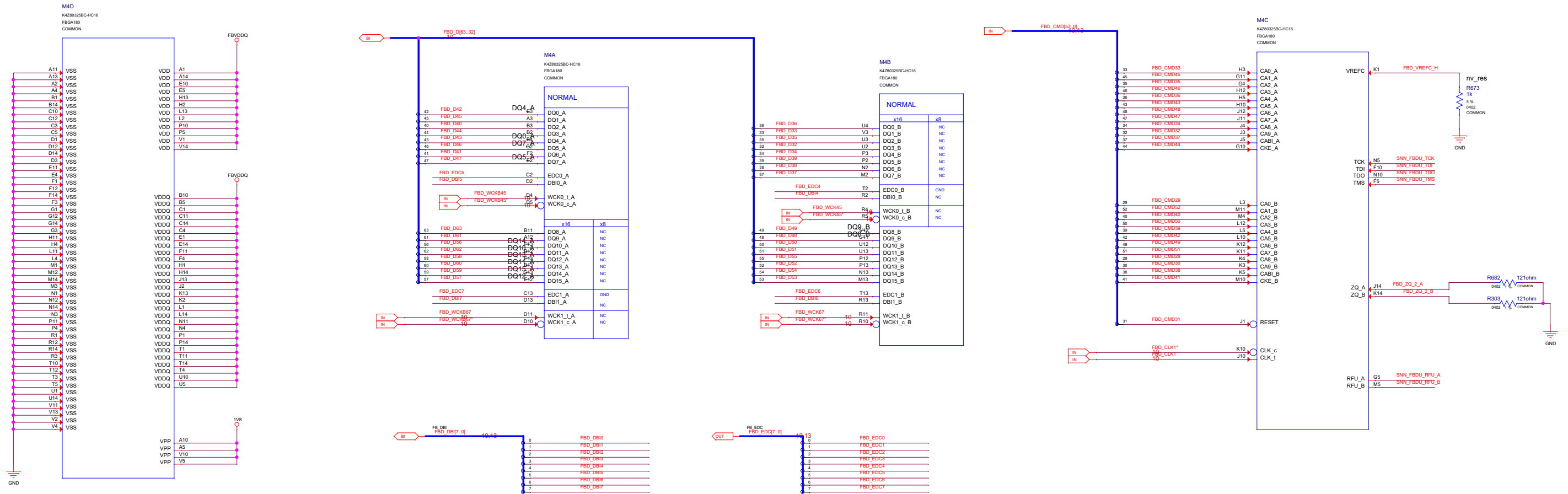
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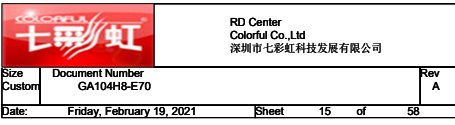


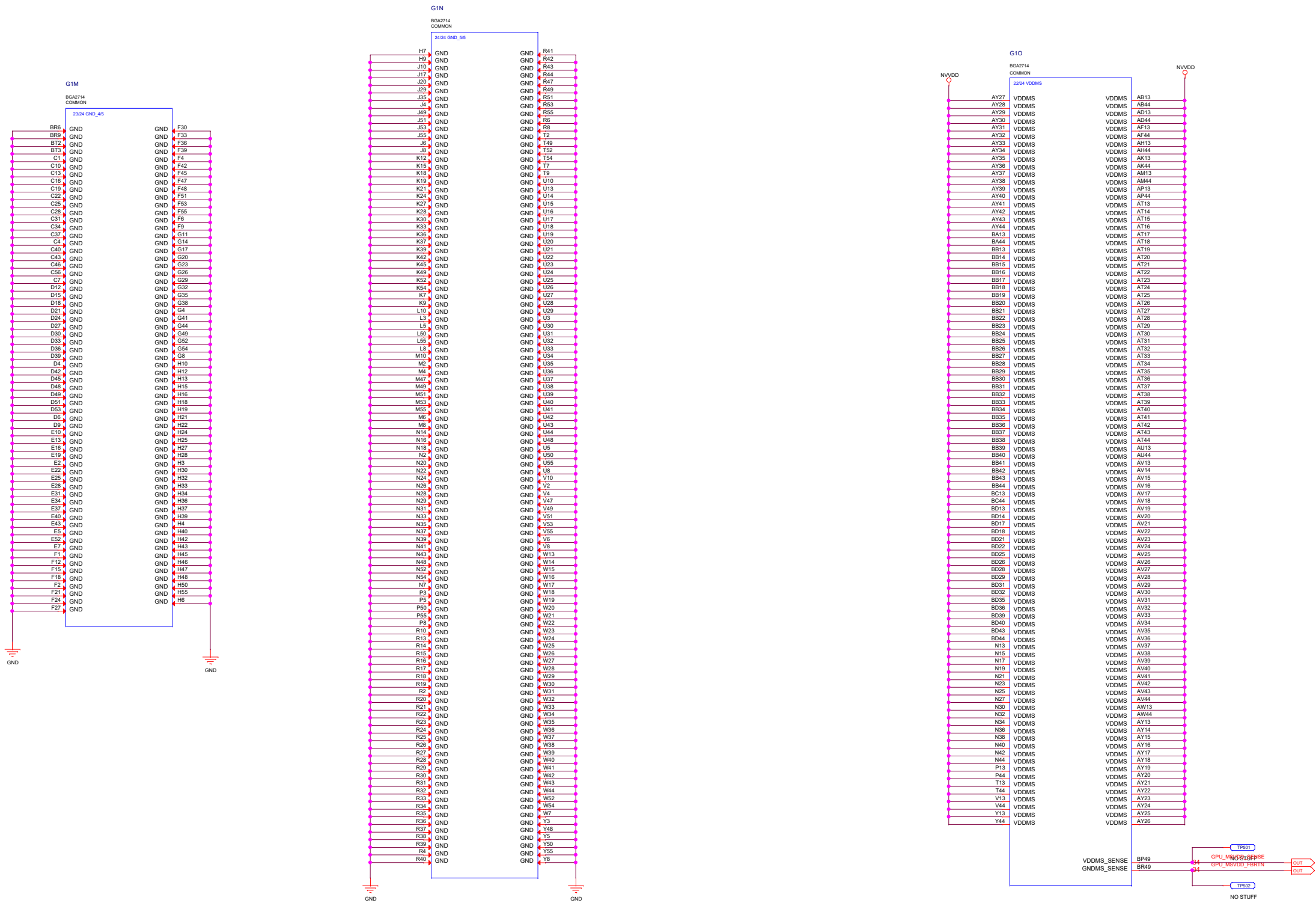


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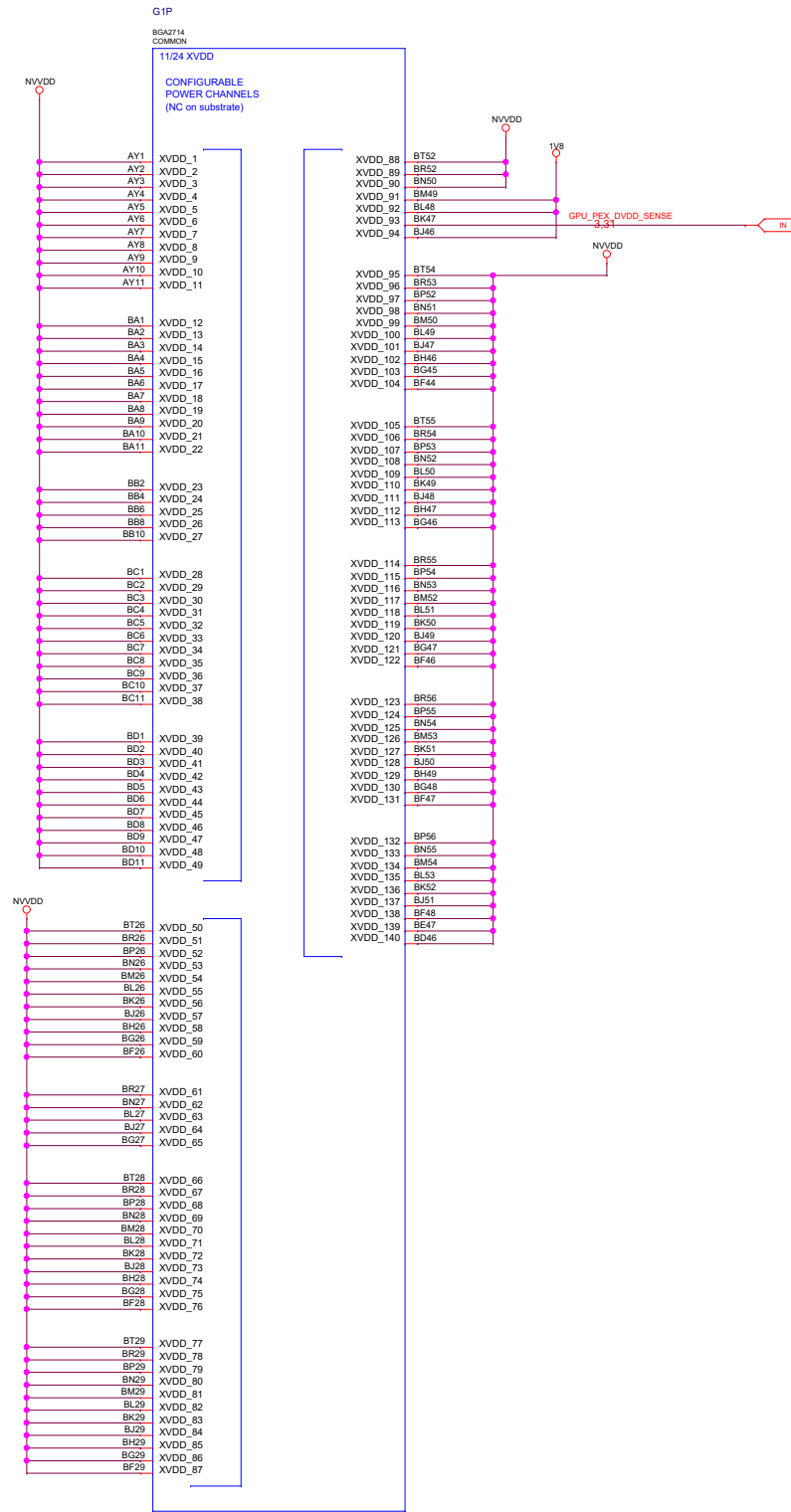







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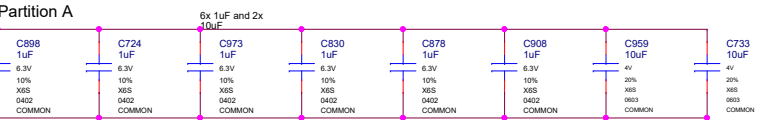
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FBVDDQ

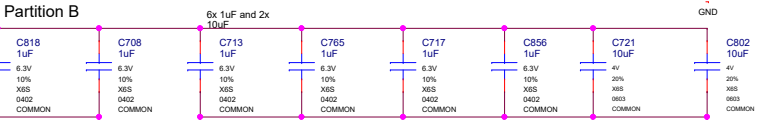
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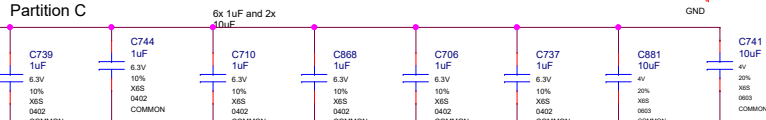
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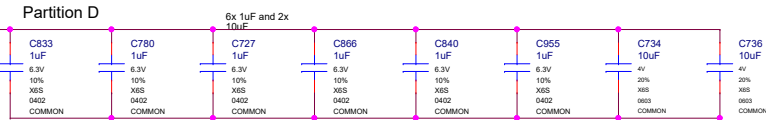
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Partition C



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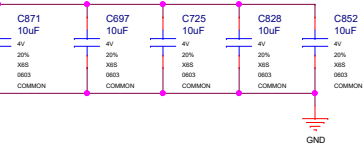


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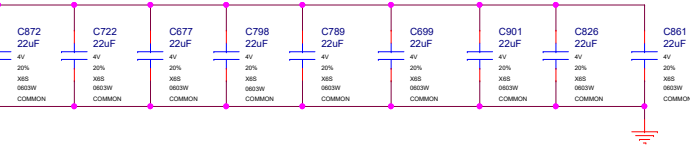
FBVDDQ

5x 0603 10uF; 9X 0603 22uF

5x 10uF



9x 22uF




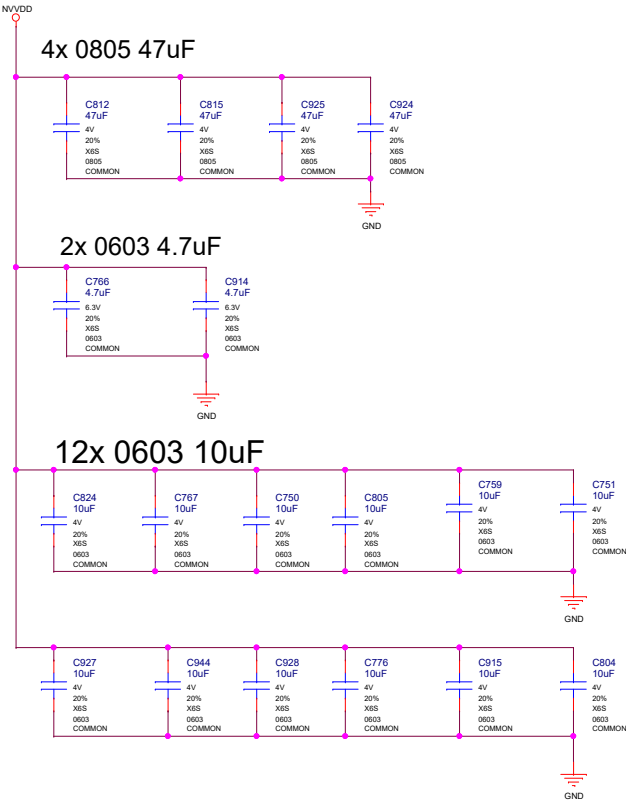
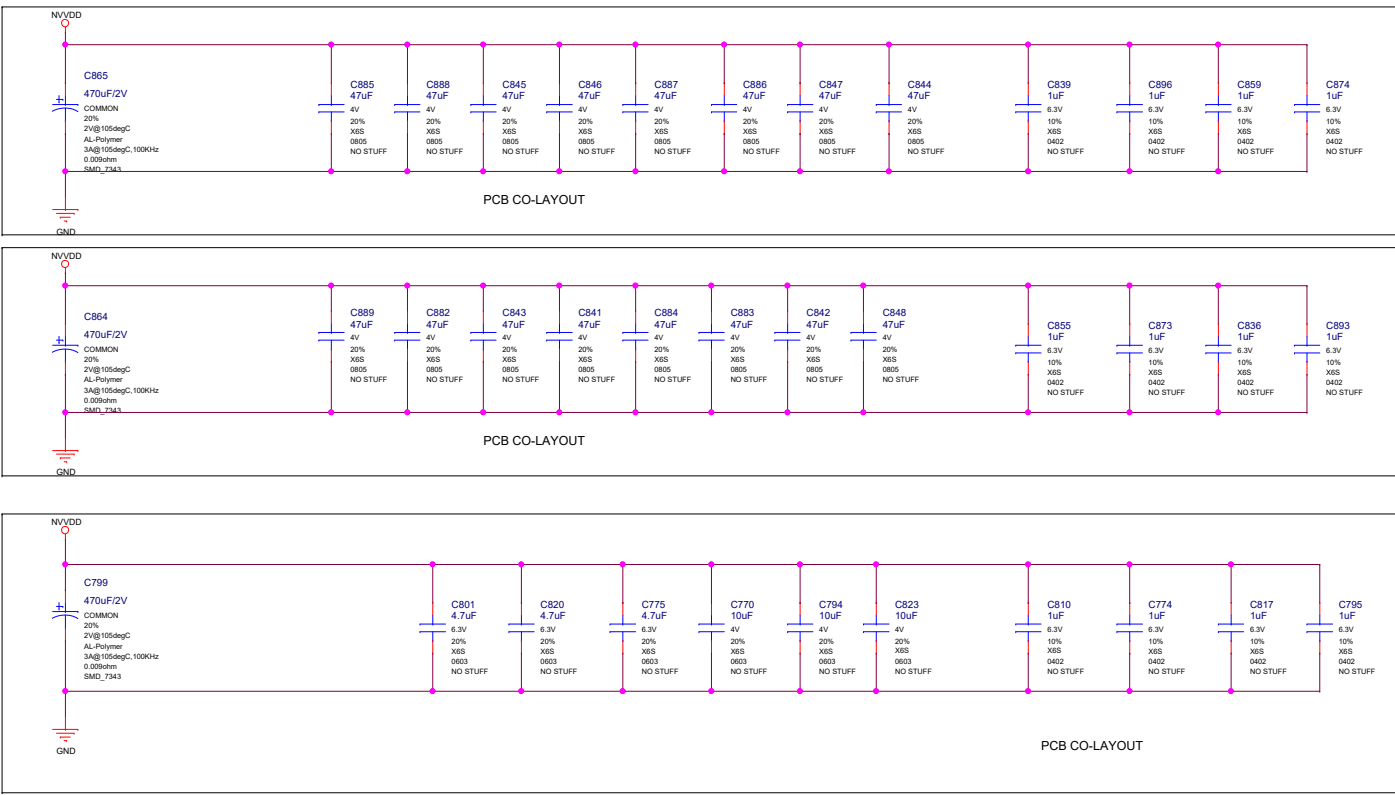
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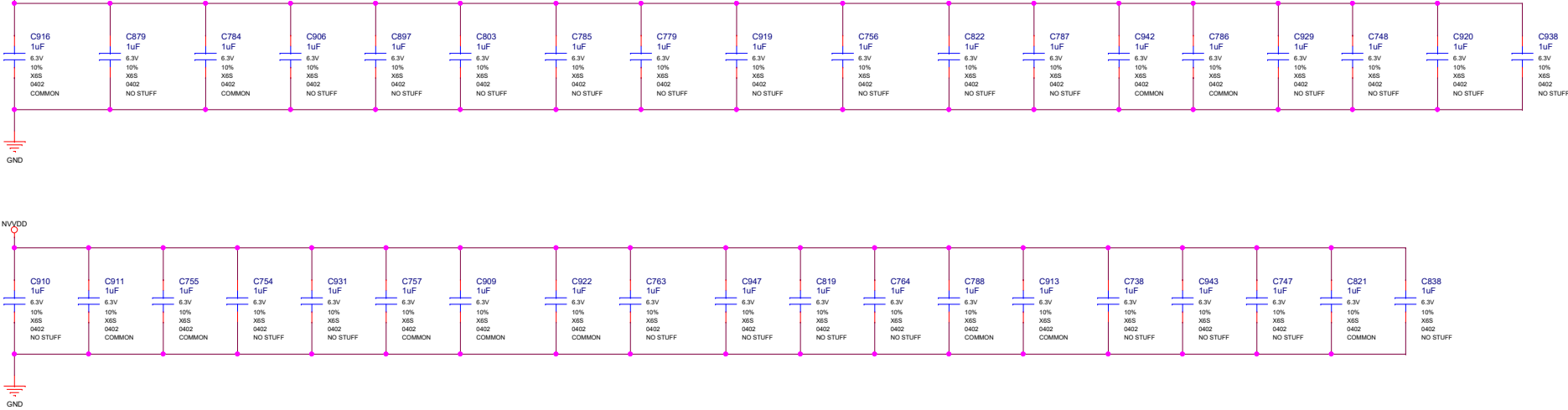
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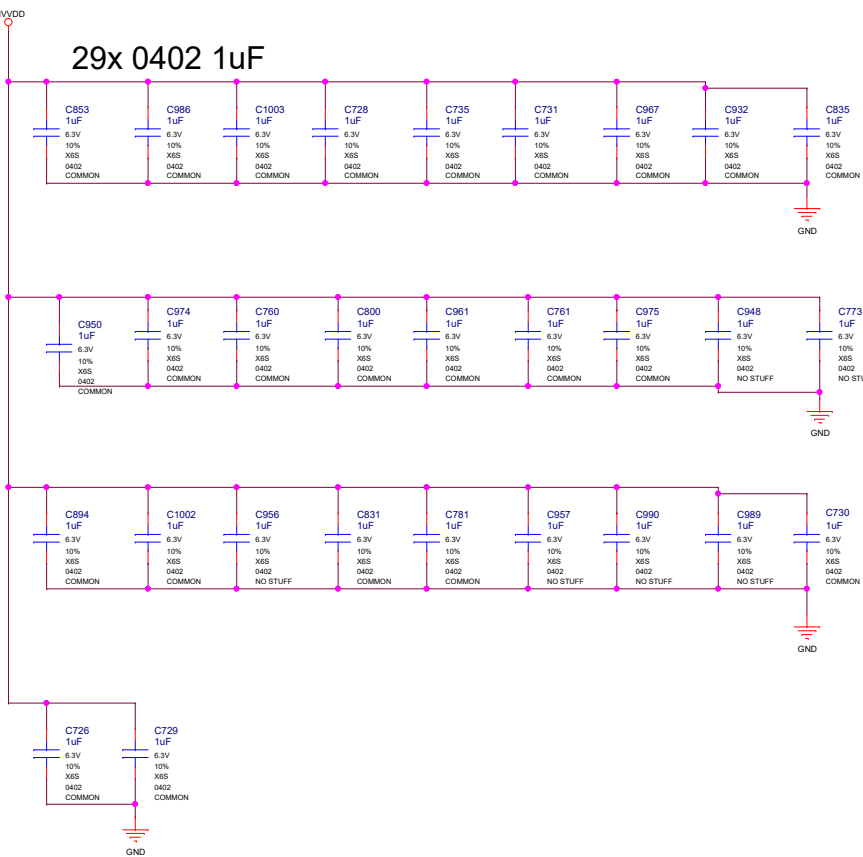
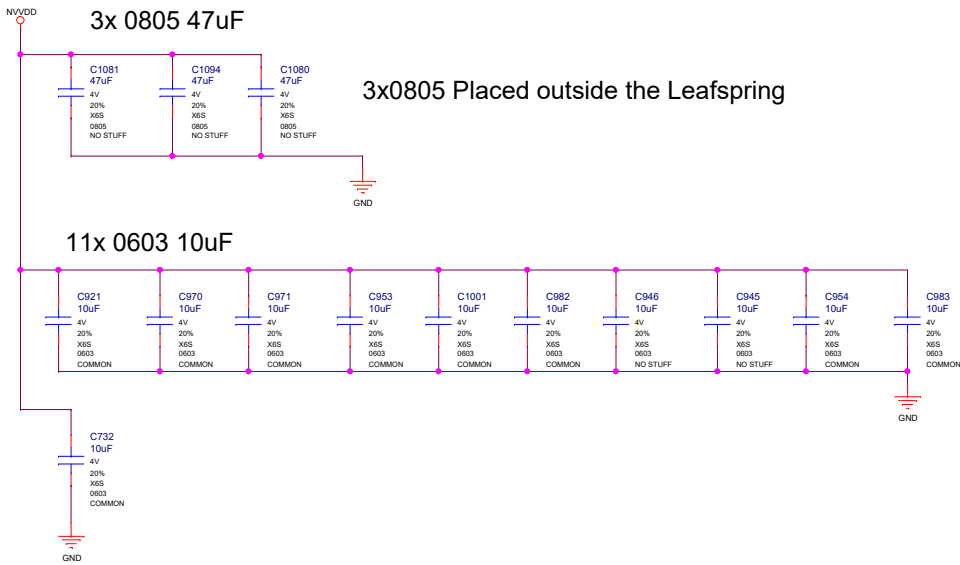
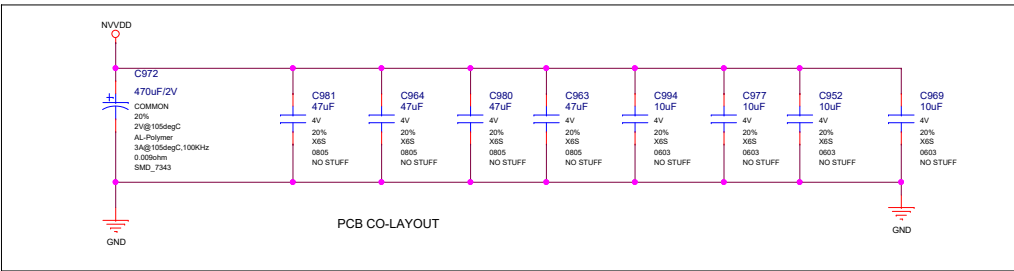
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UNDER GPU


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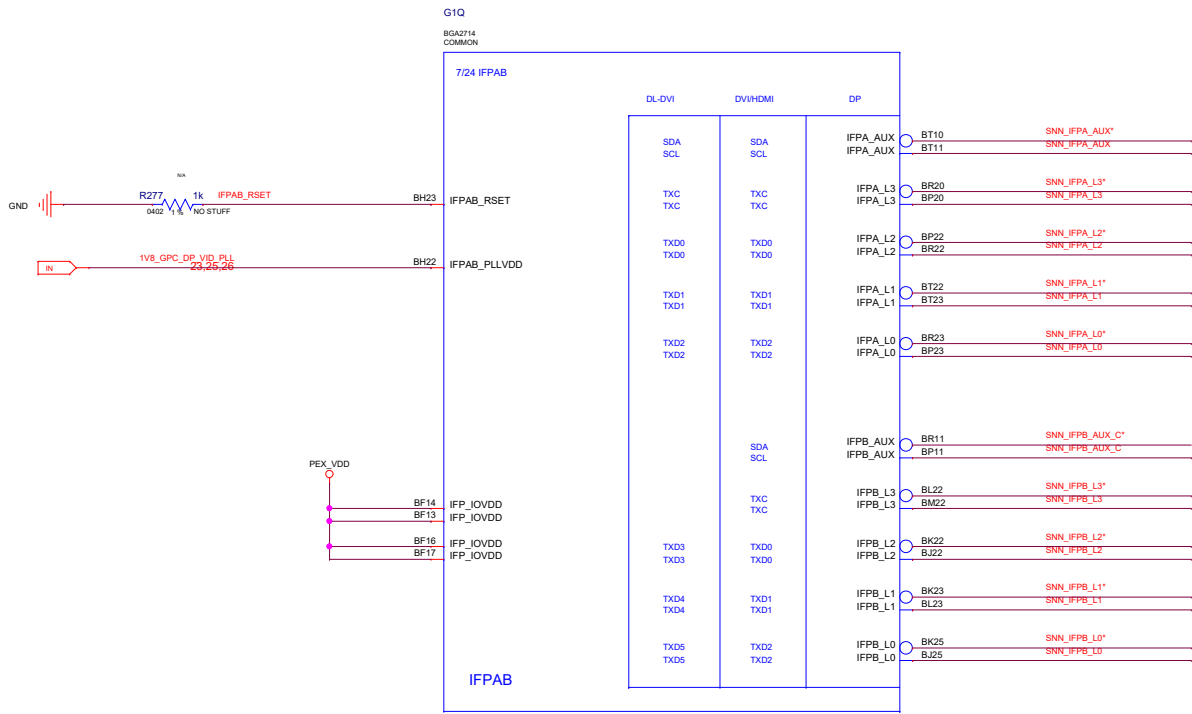


UNDER GPU

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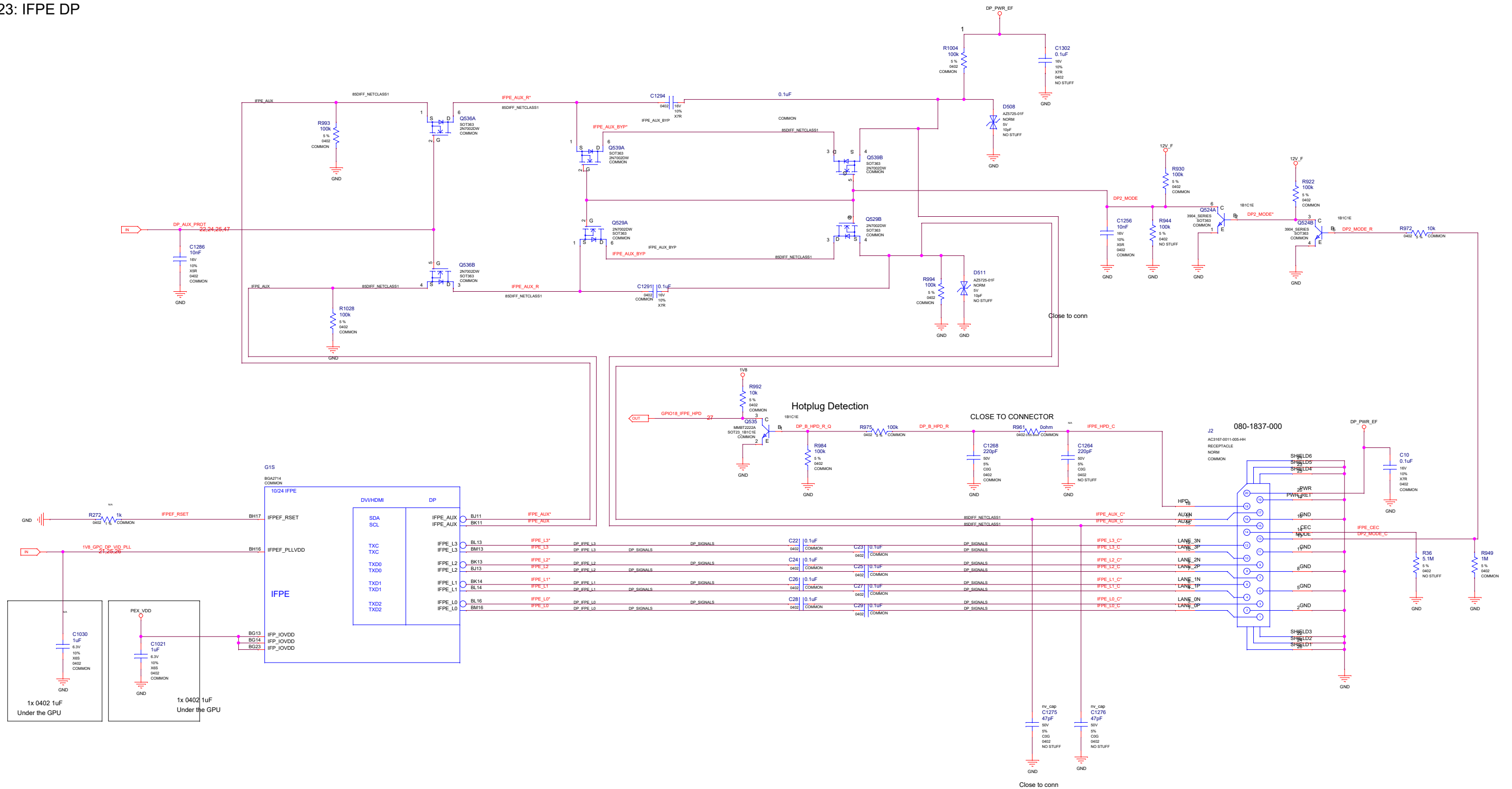
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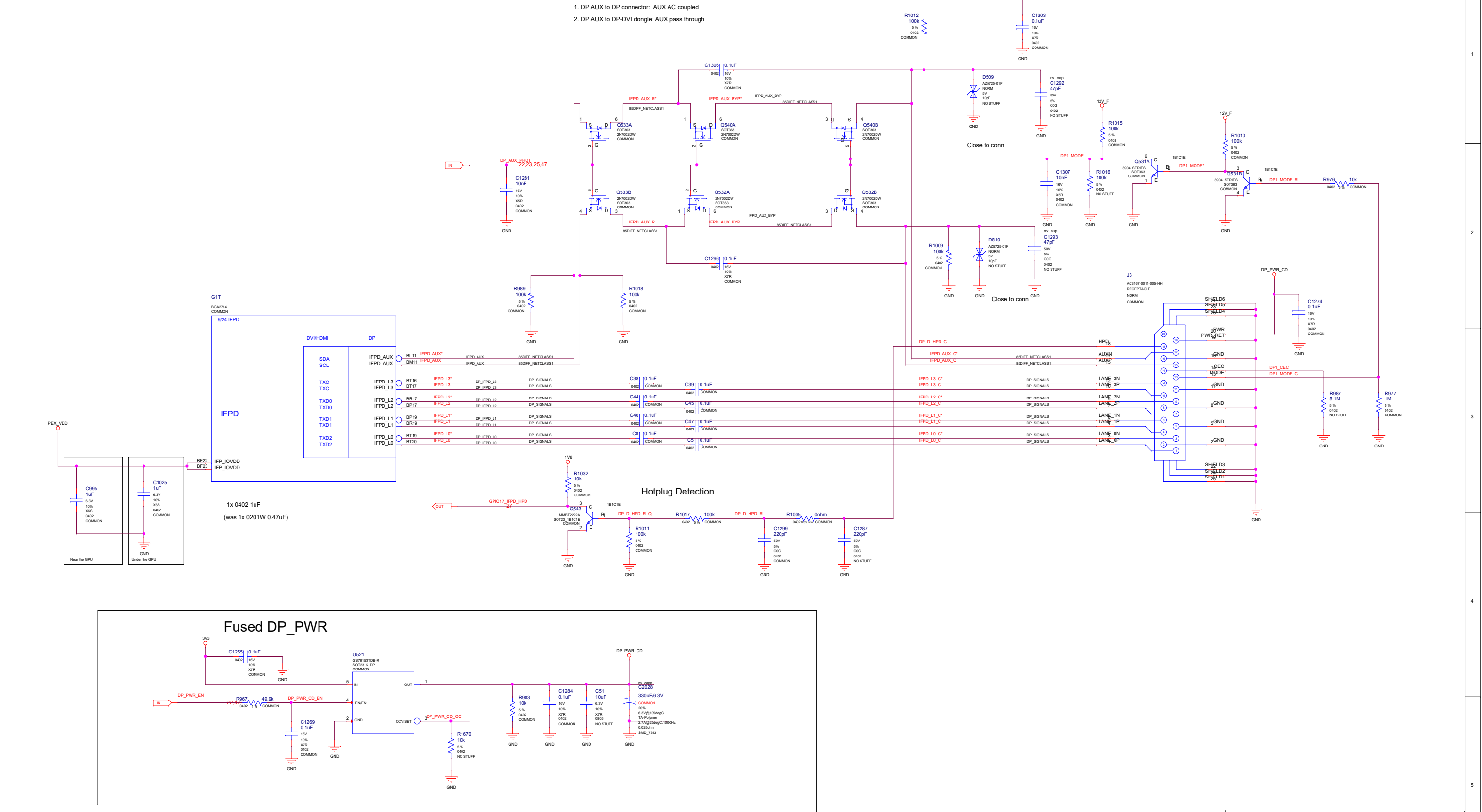
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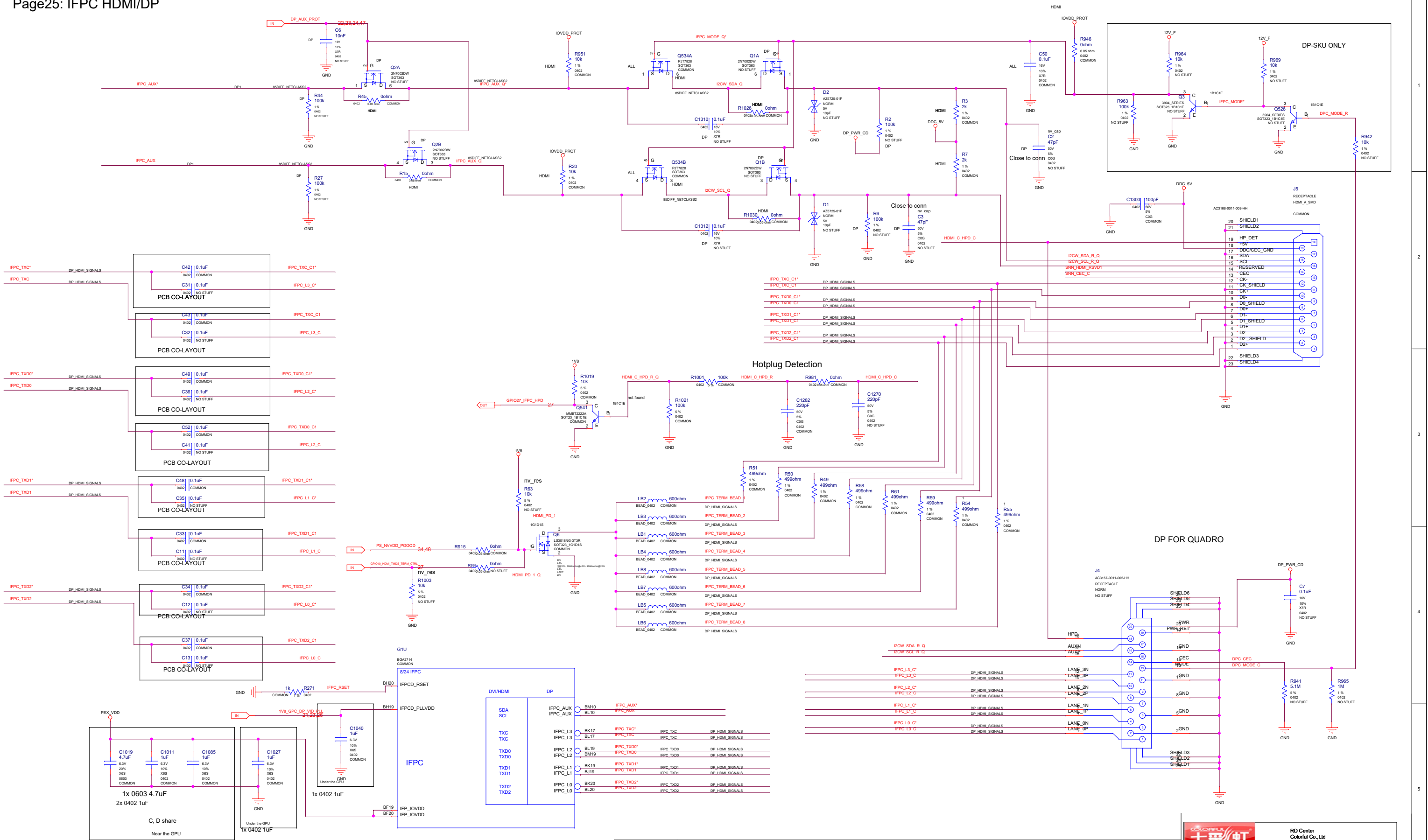
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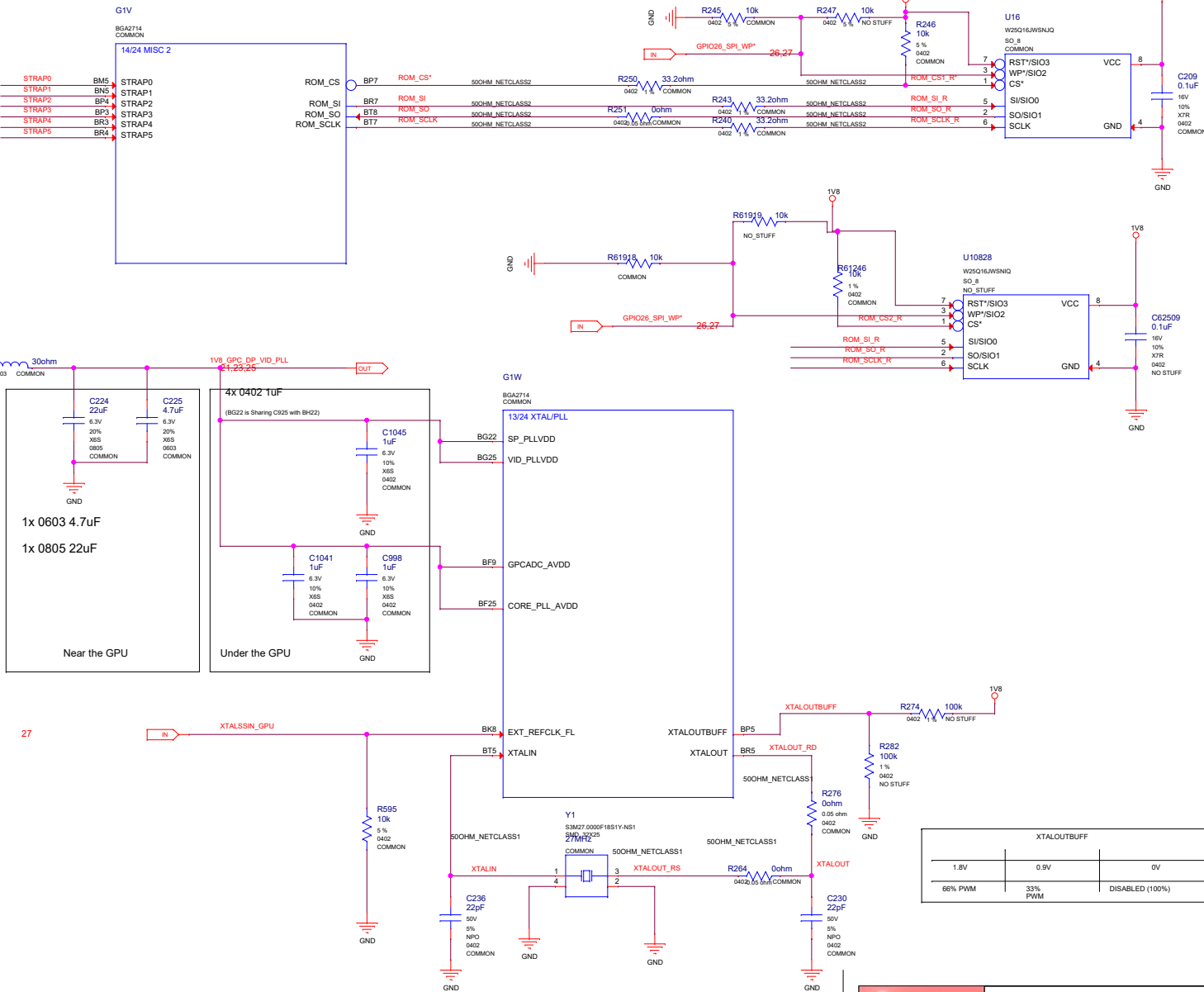


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H	H	H	0111	FS_OVERT ENABLE		
H	H	M	0000	FS_OVERT DISABLE		
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0


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1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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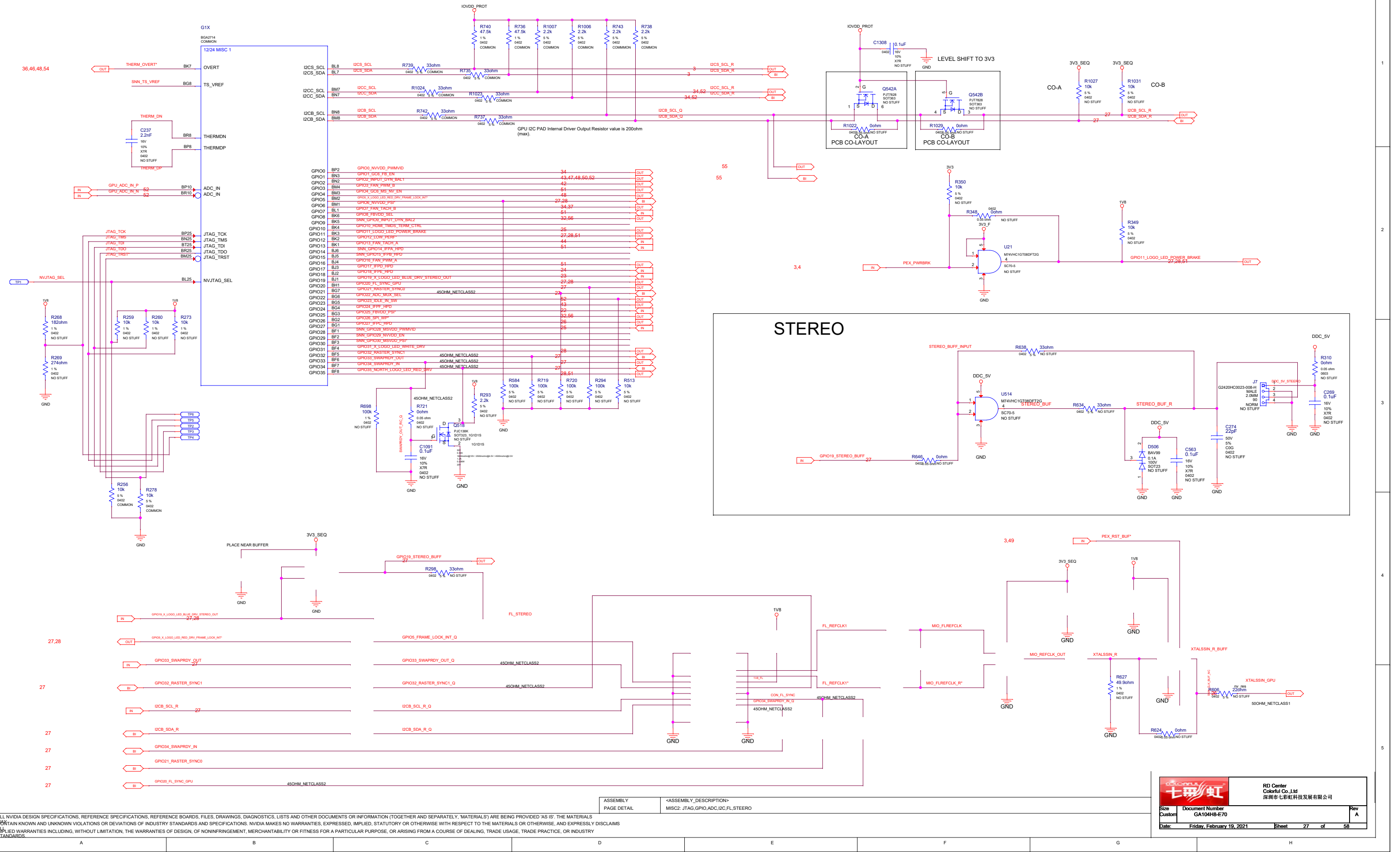
DEFAULT



XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

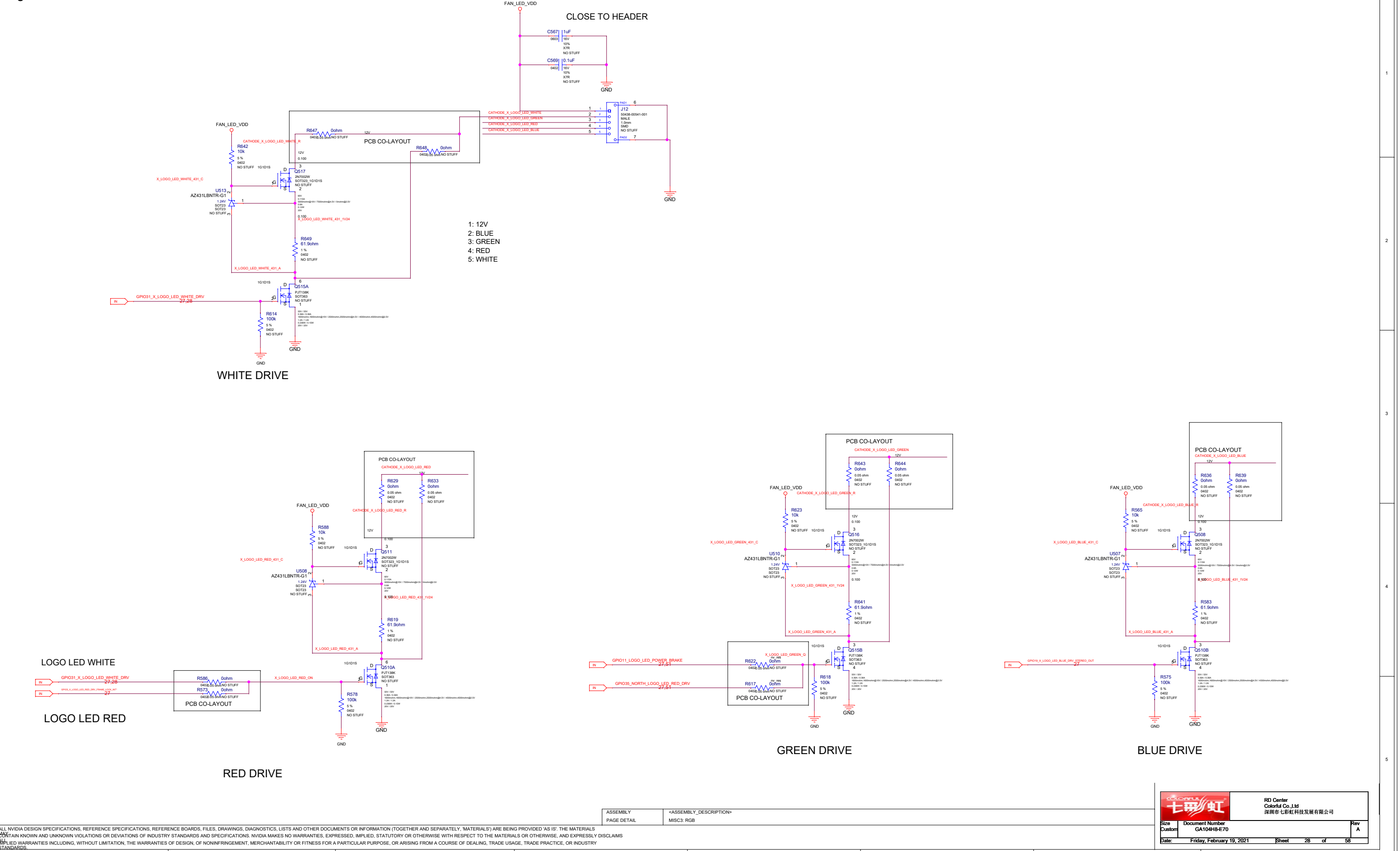
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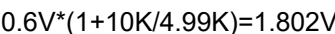


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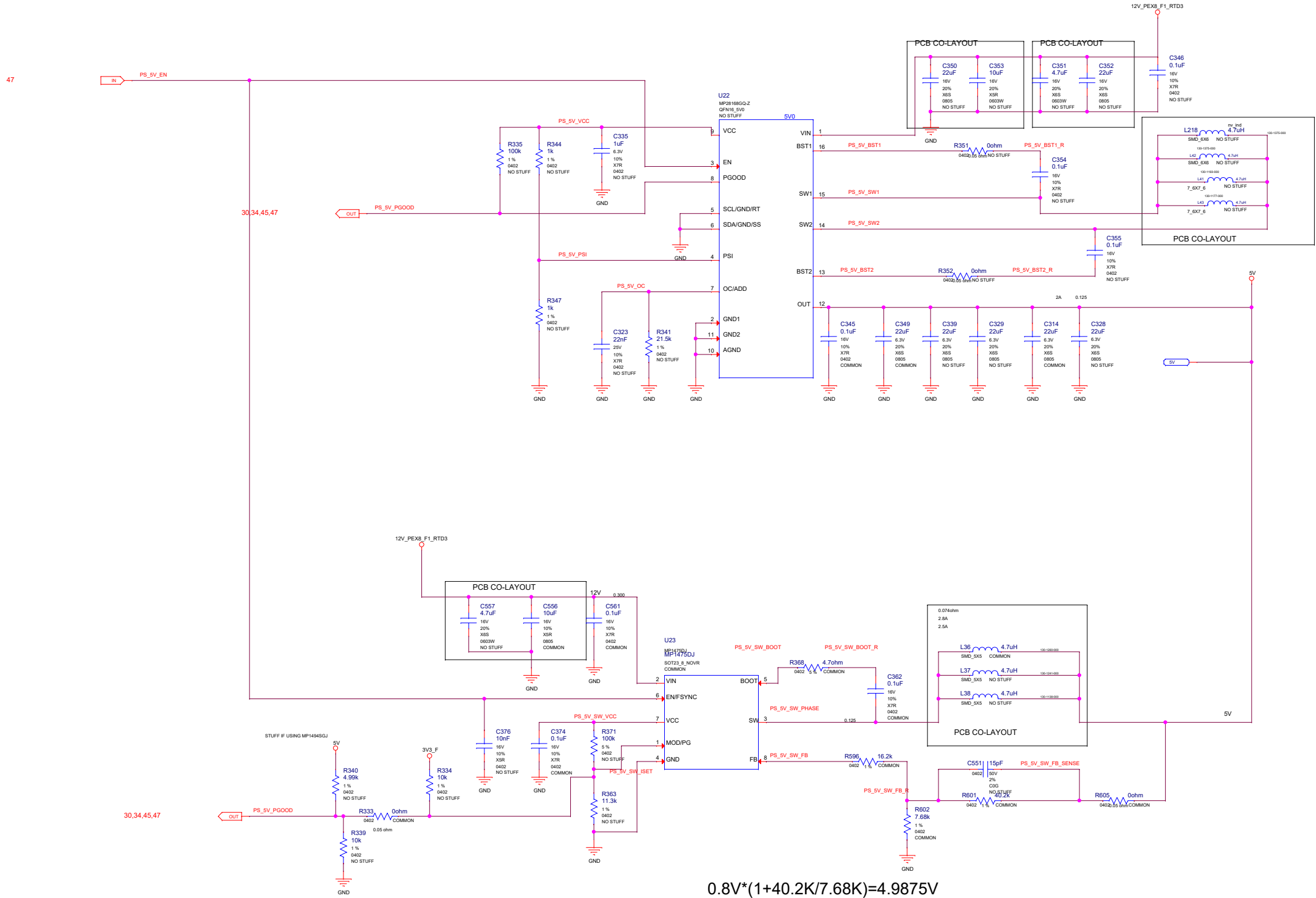
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## 0.6V




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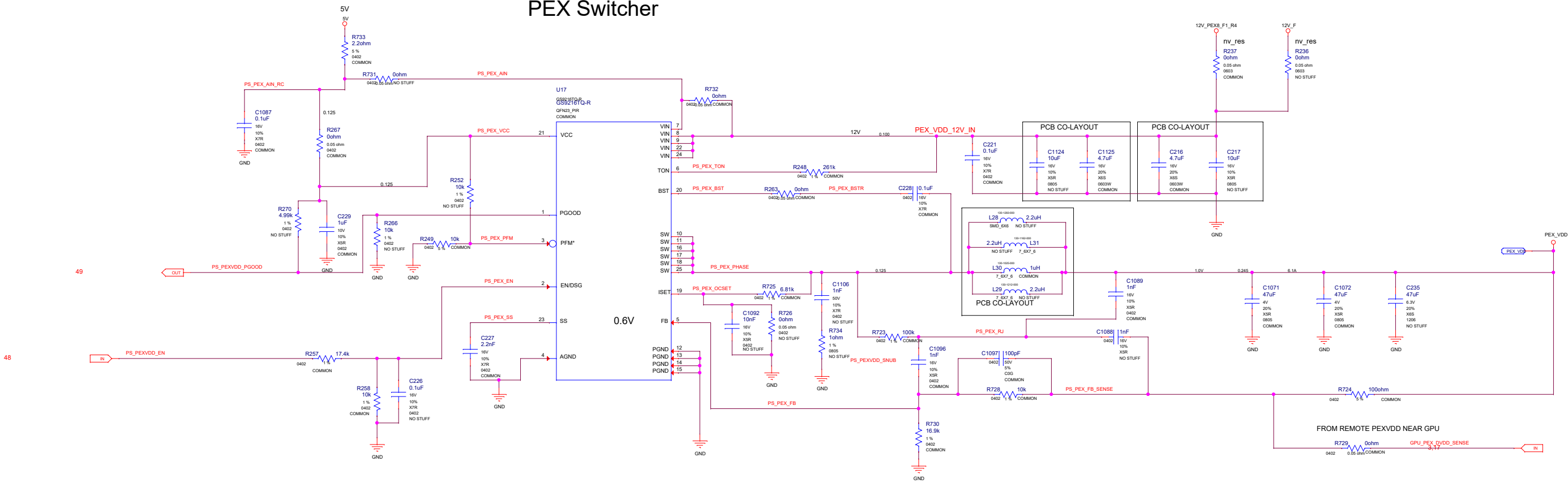


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ASSEMBLY PAGE DETAIL <ASSEMBLY\_DESCRIPTION> PS: 5V

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PEX Switcher

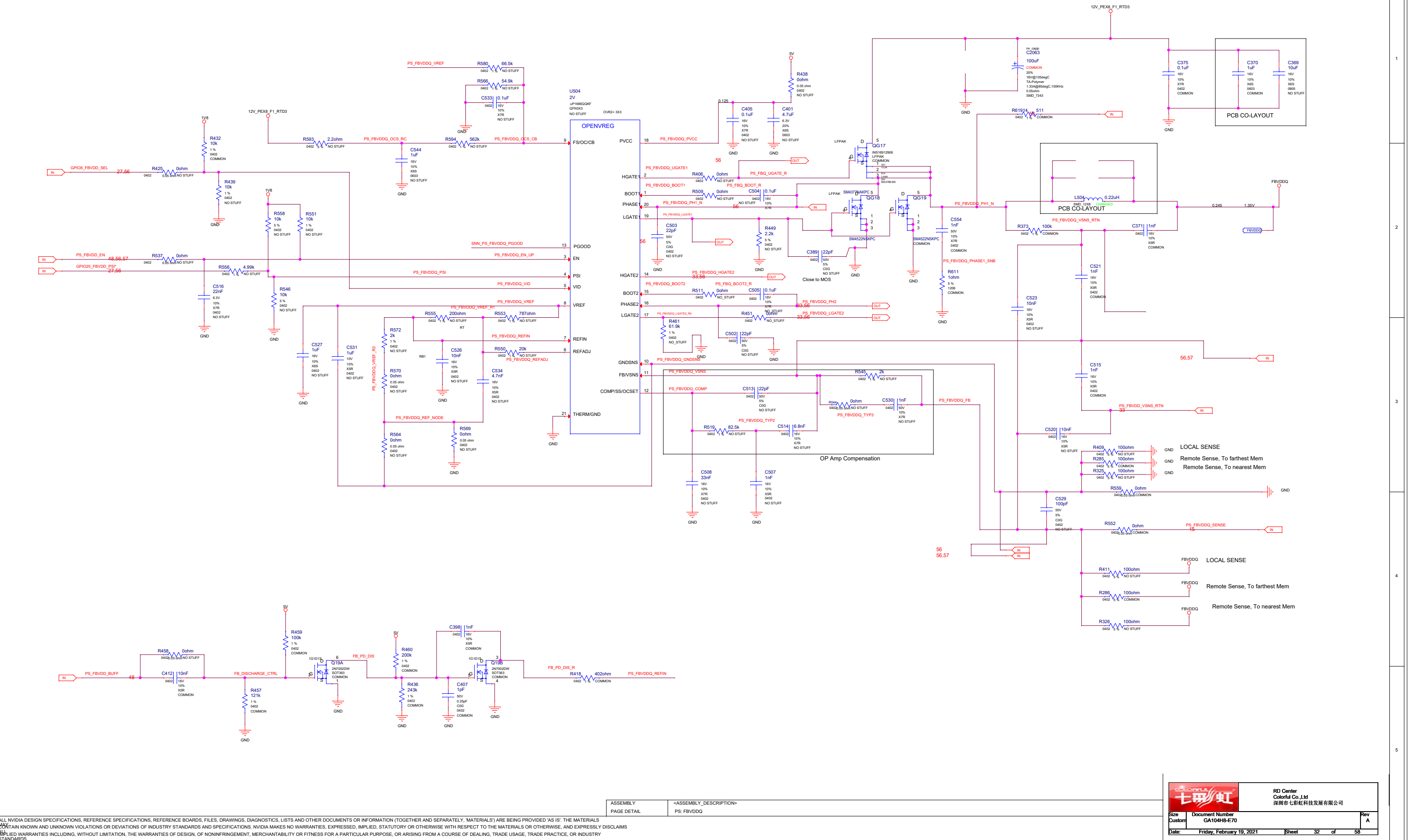


$0.6V \cdot (1 + 10K/16.9K) = 0.955V$

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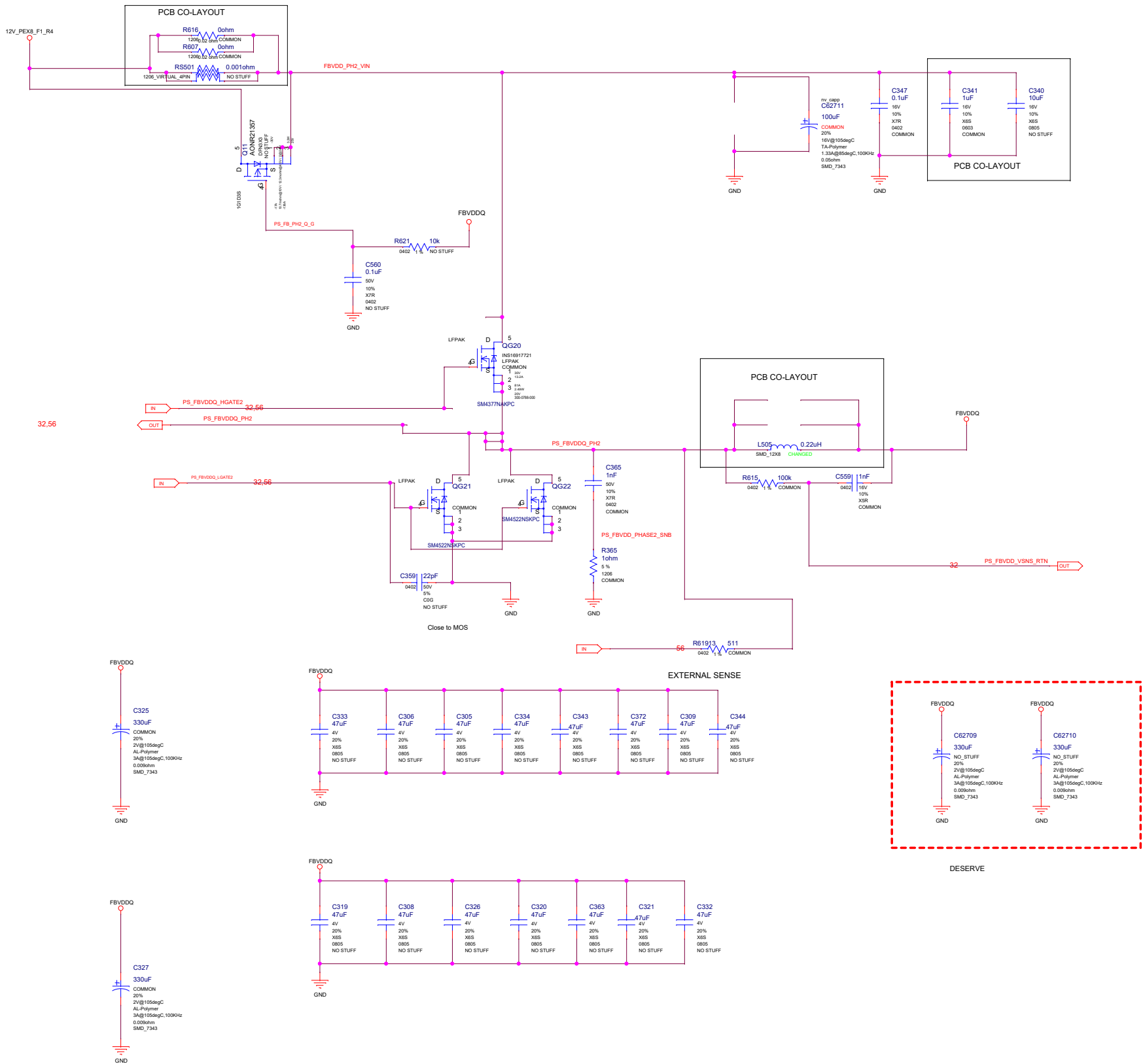
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FBVDD PH2 INPUT ANTI-BACKDRIVE



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ASSEMBLY PAGE DETAIL <ASSEMBLY\_DESCRIPTION> PS: FBVDDQ PH2

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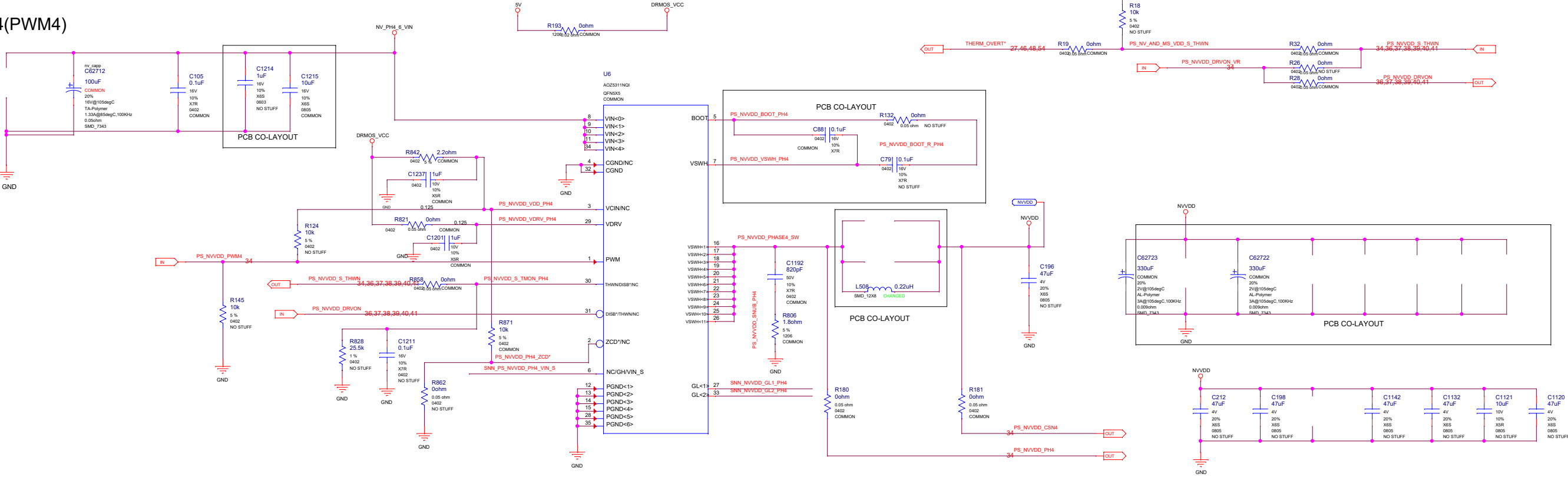


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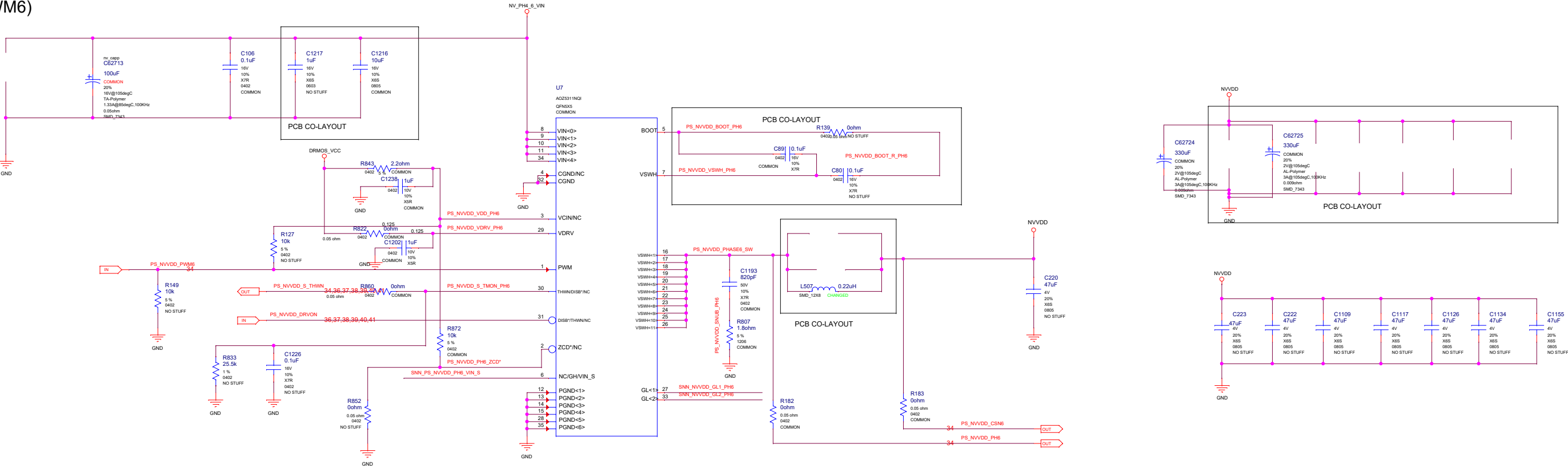
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NVVDD PH4(PWM4)



NVVDD PH6(PWM6)



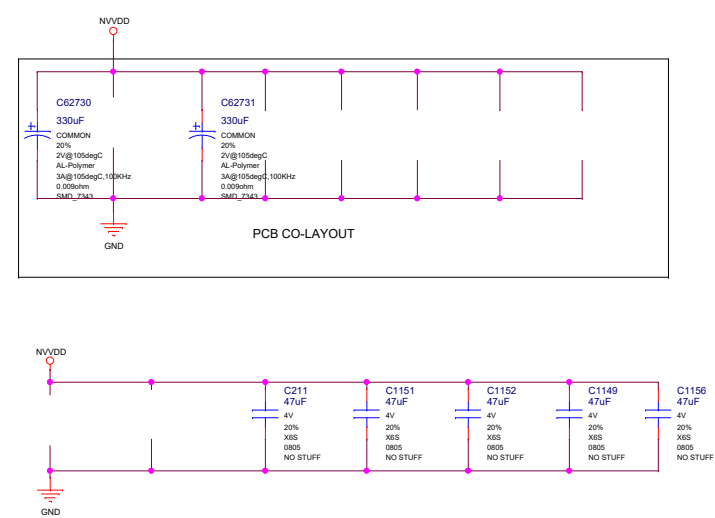
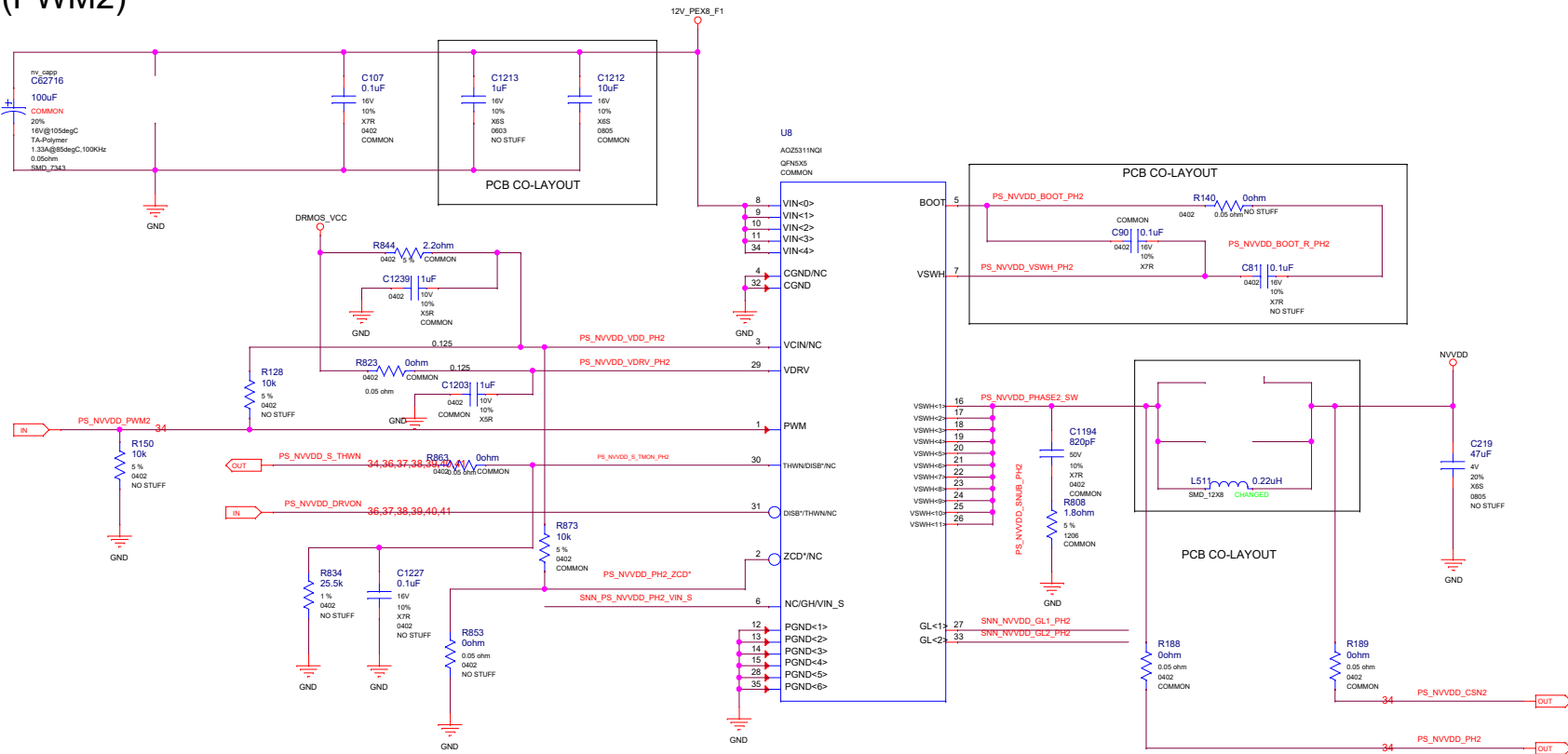
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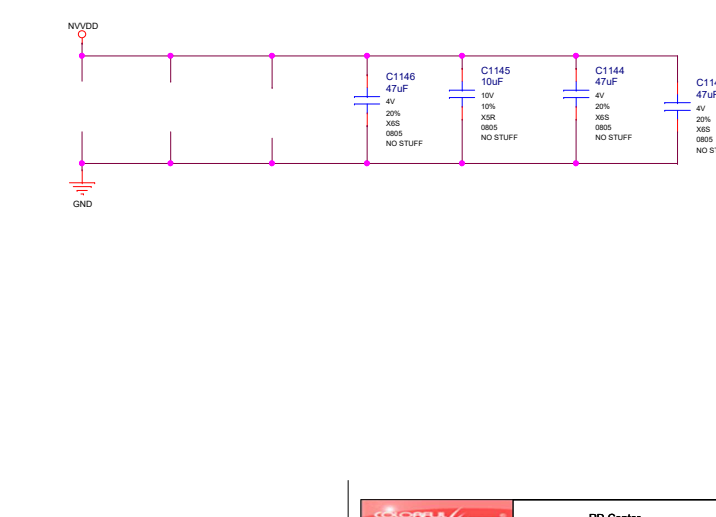
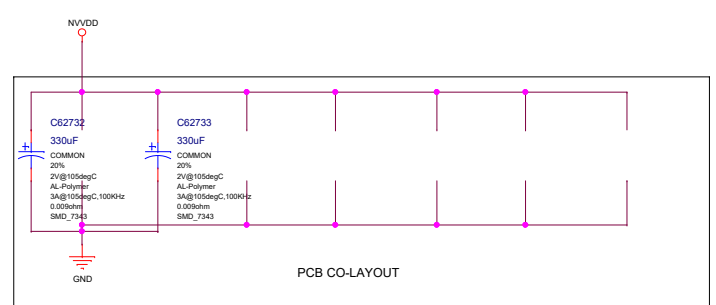
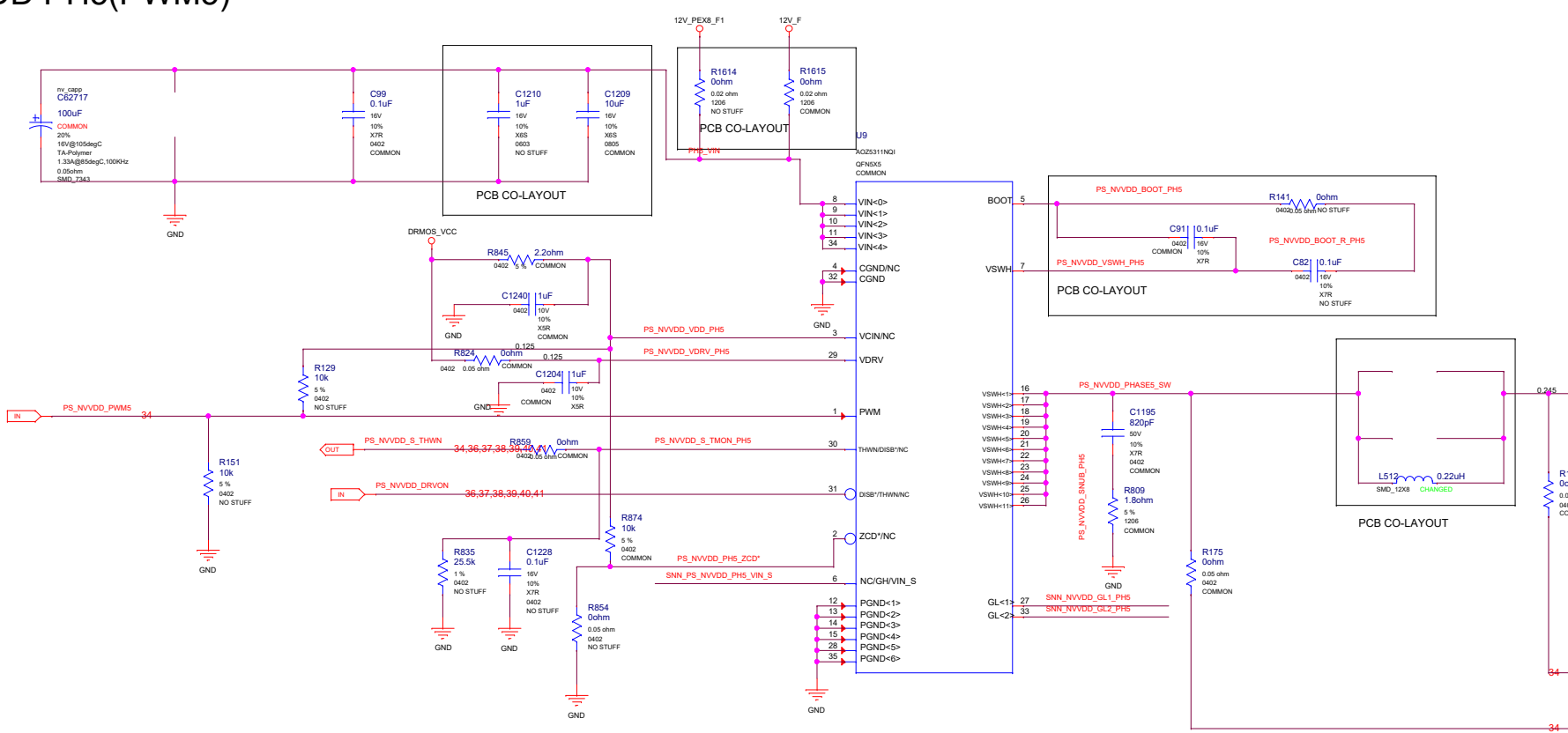
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NVVDD PH2(PWM2)




NVVDD PH5(PWM5)



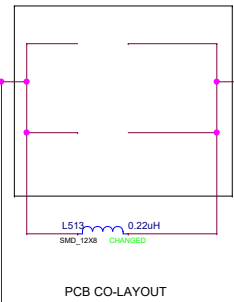
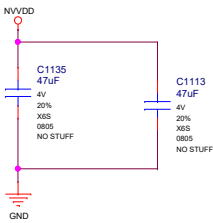
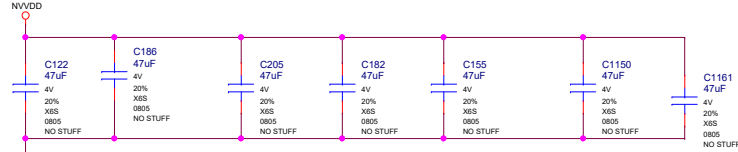
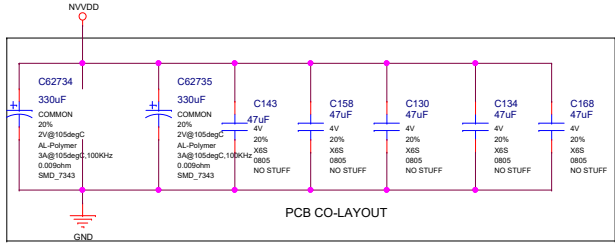
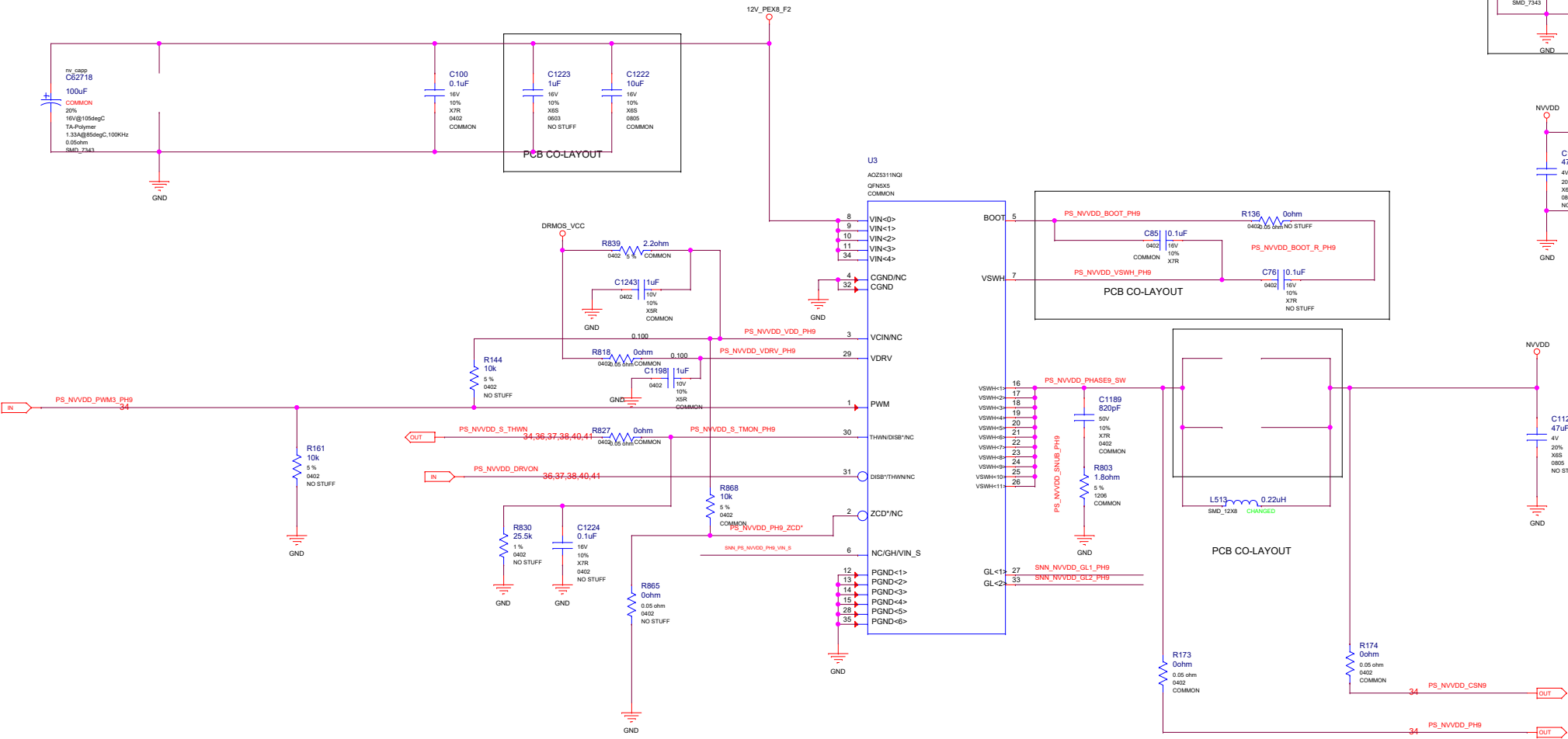
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ASSEMBLY PAGE DETAIL	<ASSEMBLY_DESCRIPTION> PS: NVVDD PH2, PH5
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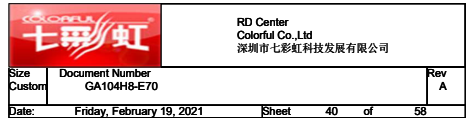


NVVDD PH9(PWM3)



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1

2

3

4

5

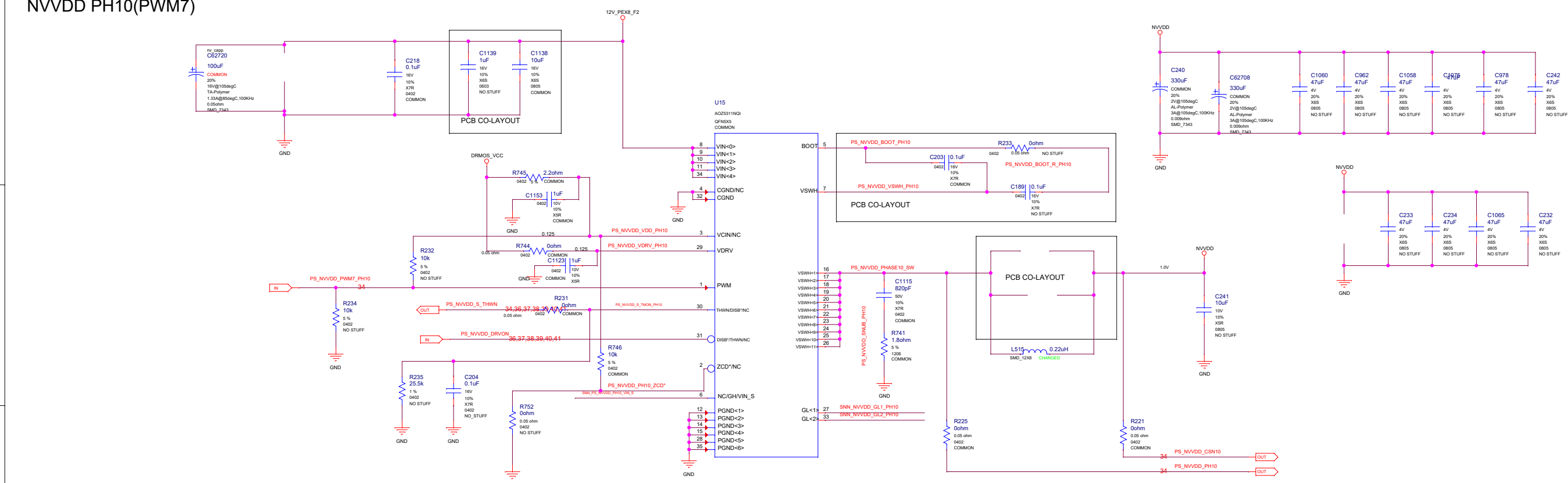
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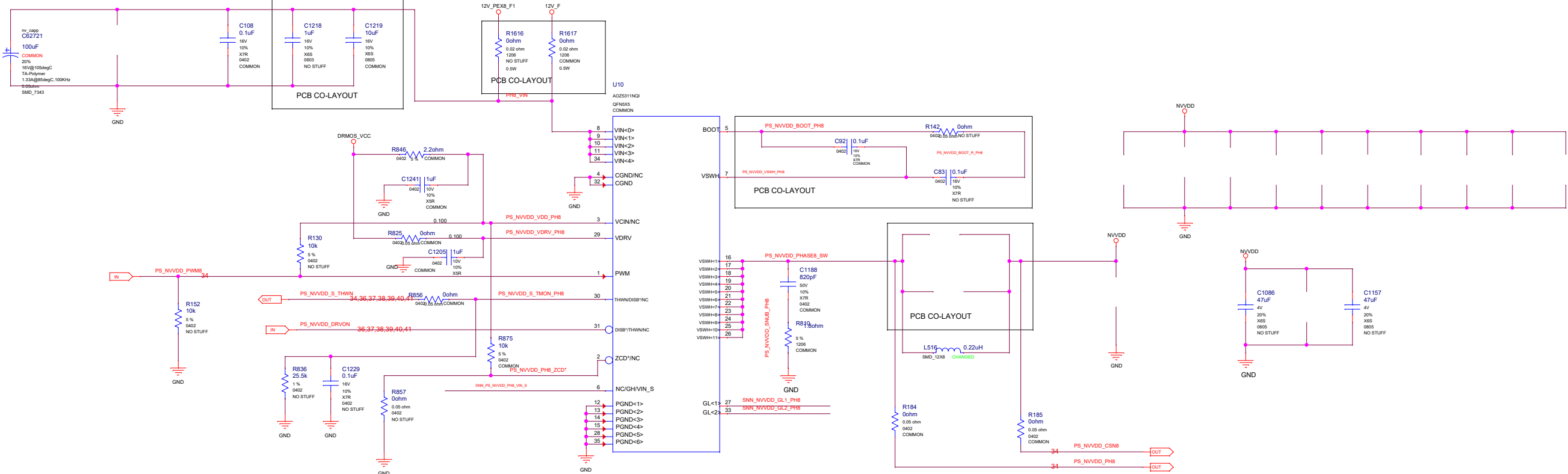
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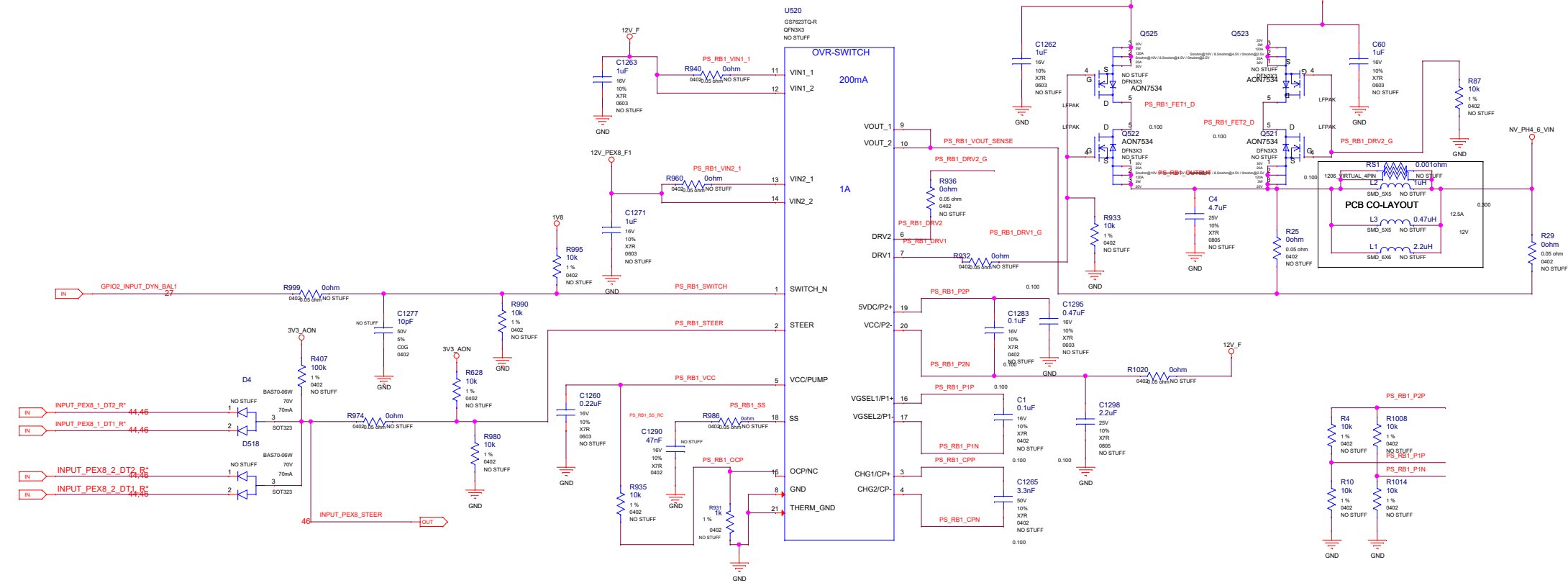
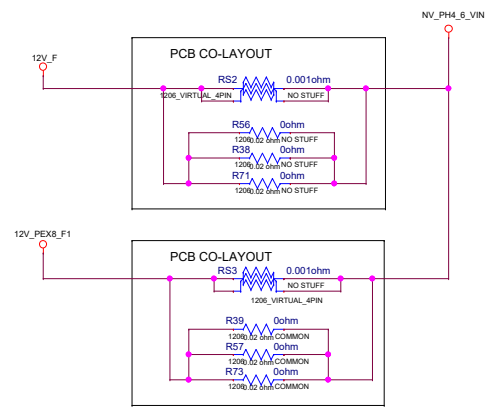
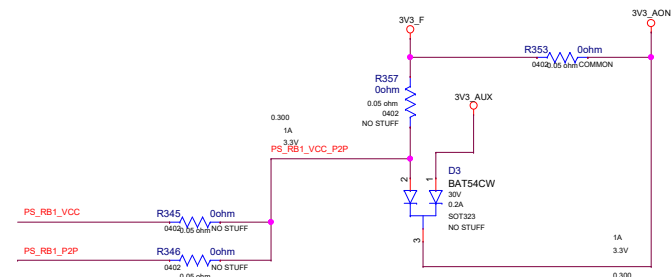
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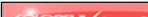
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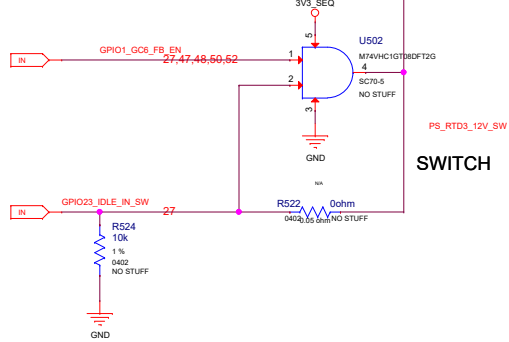
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## Page42: Input Power Balancing Switcher

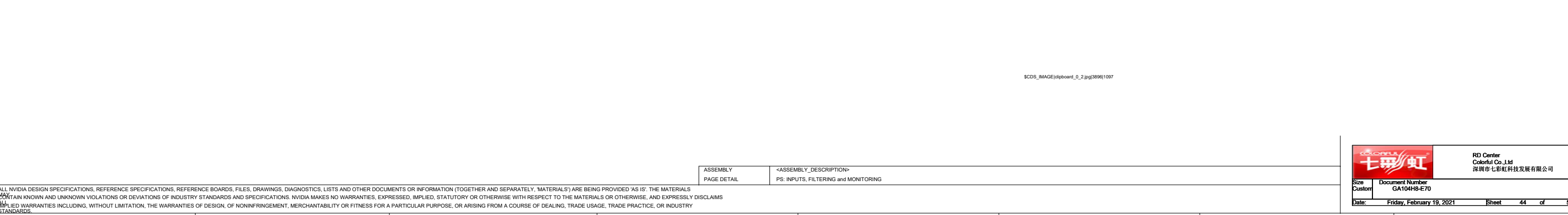
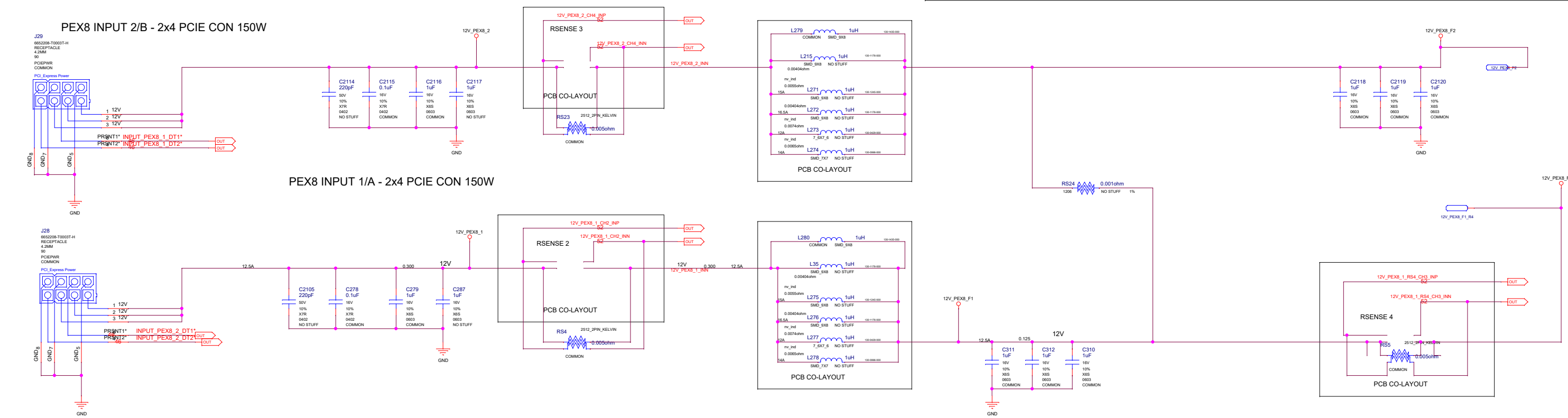
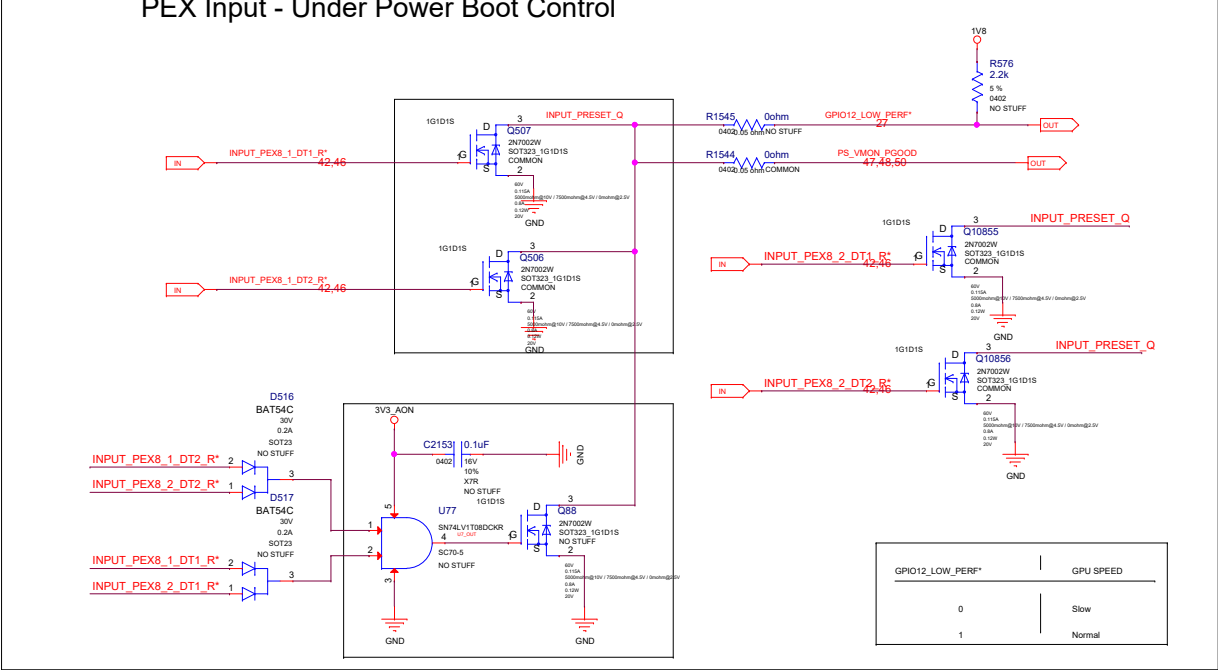
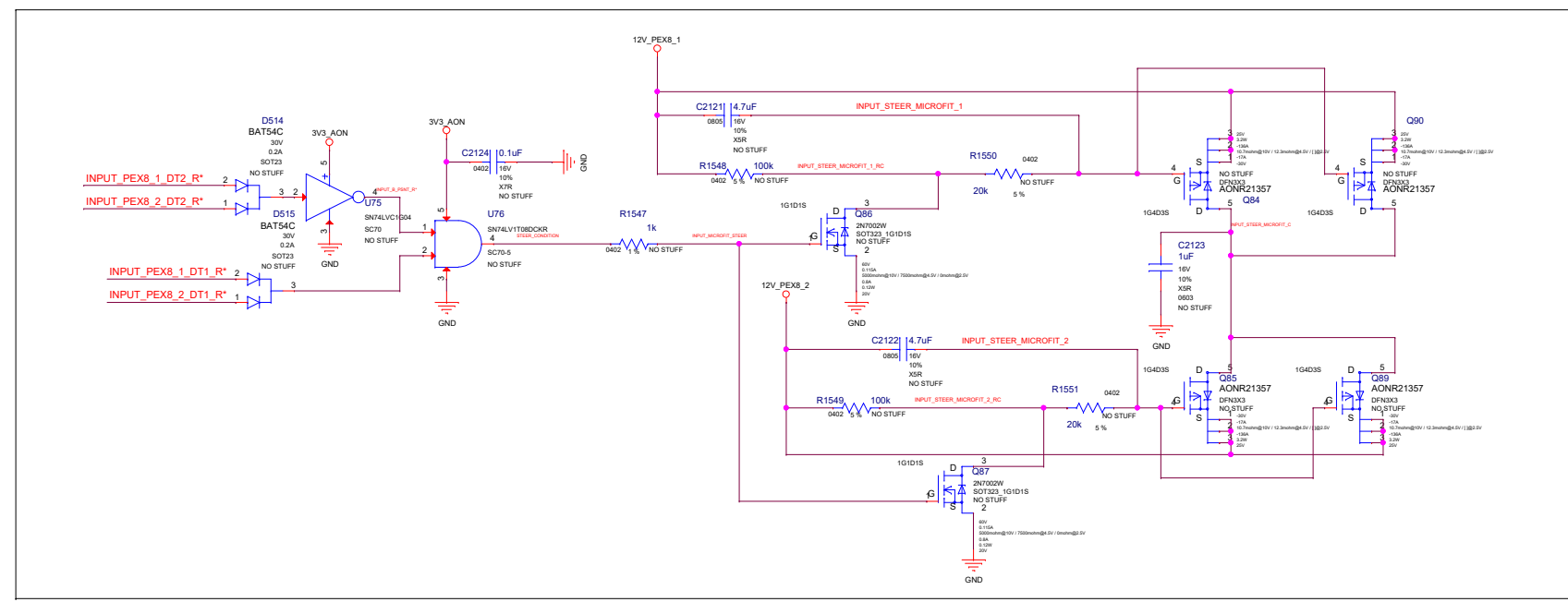


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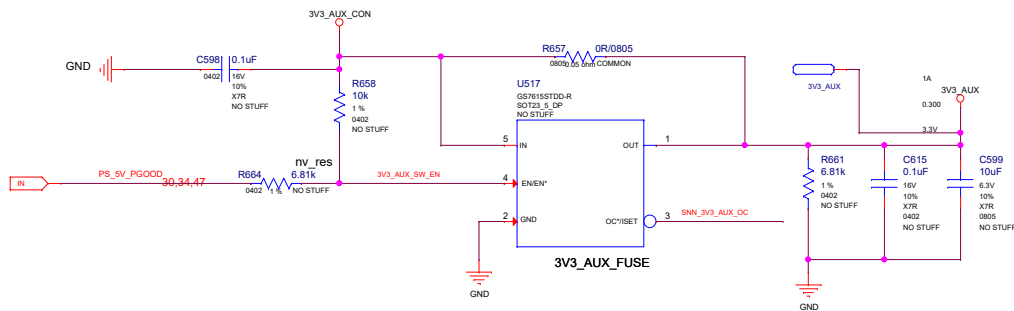
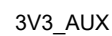
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AND GATE LOGIC					
GPIO1	GPIO29	SWITCH	VOUT	SWITCH	VOUT
0	0	0	12V	0	VOUT = VIN1
0	1	0	12V	1	VOUT = VIN2
1	0	0	12V		
1	1	1	3V3A		



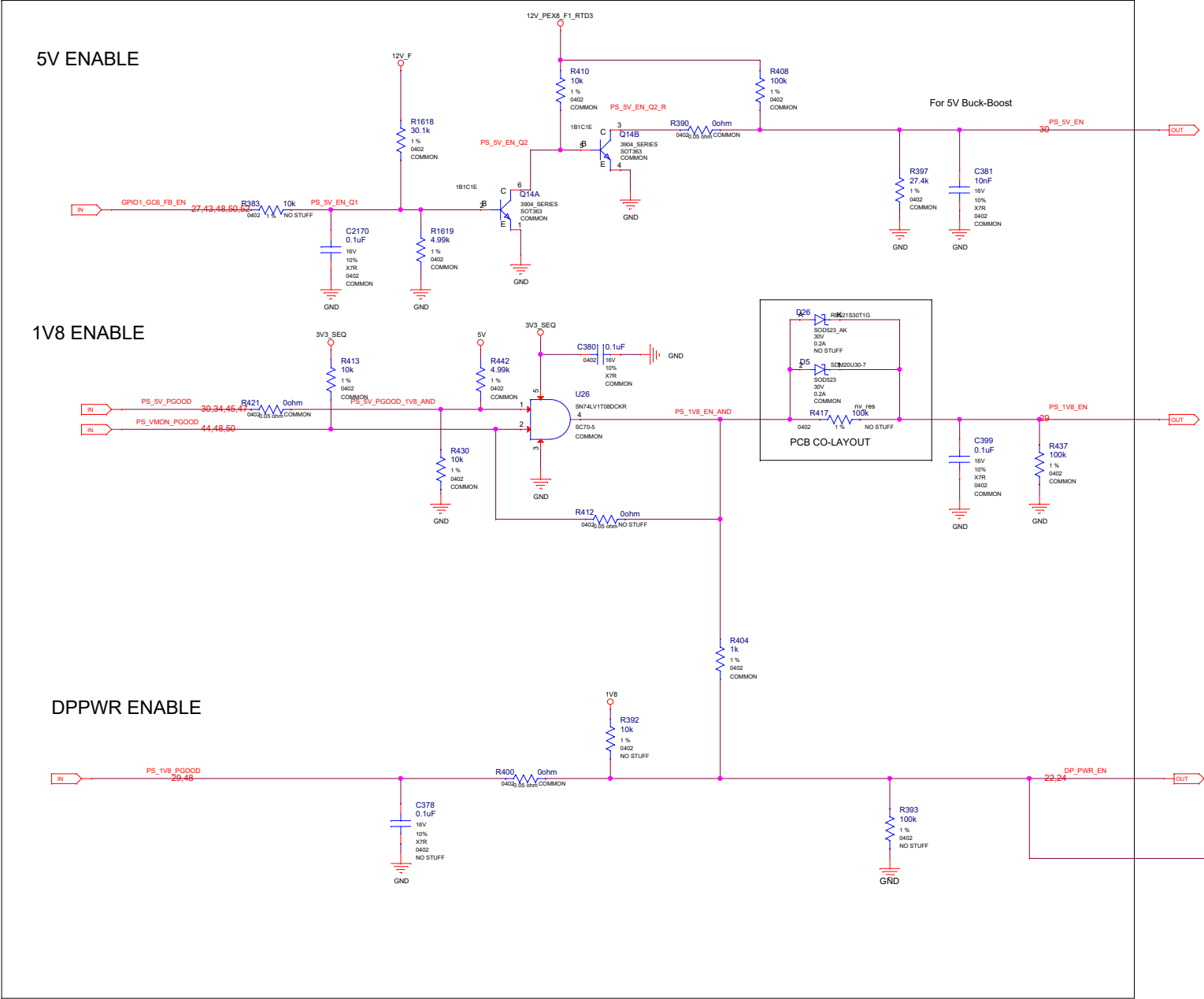




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PAGE DETAIL	PS: PEX_12V, PEX_3V3 AND A3V3_AUX

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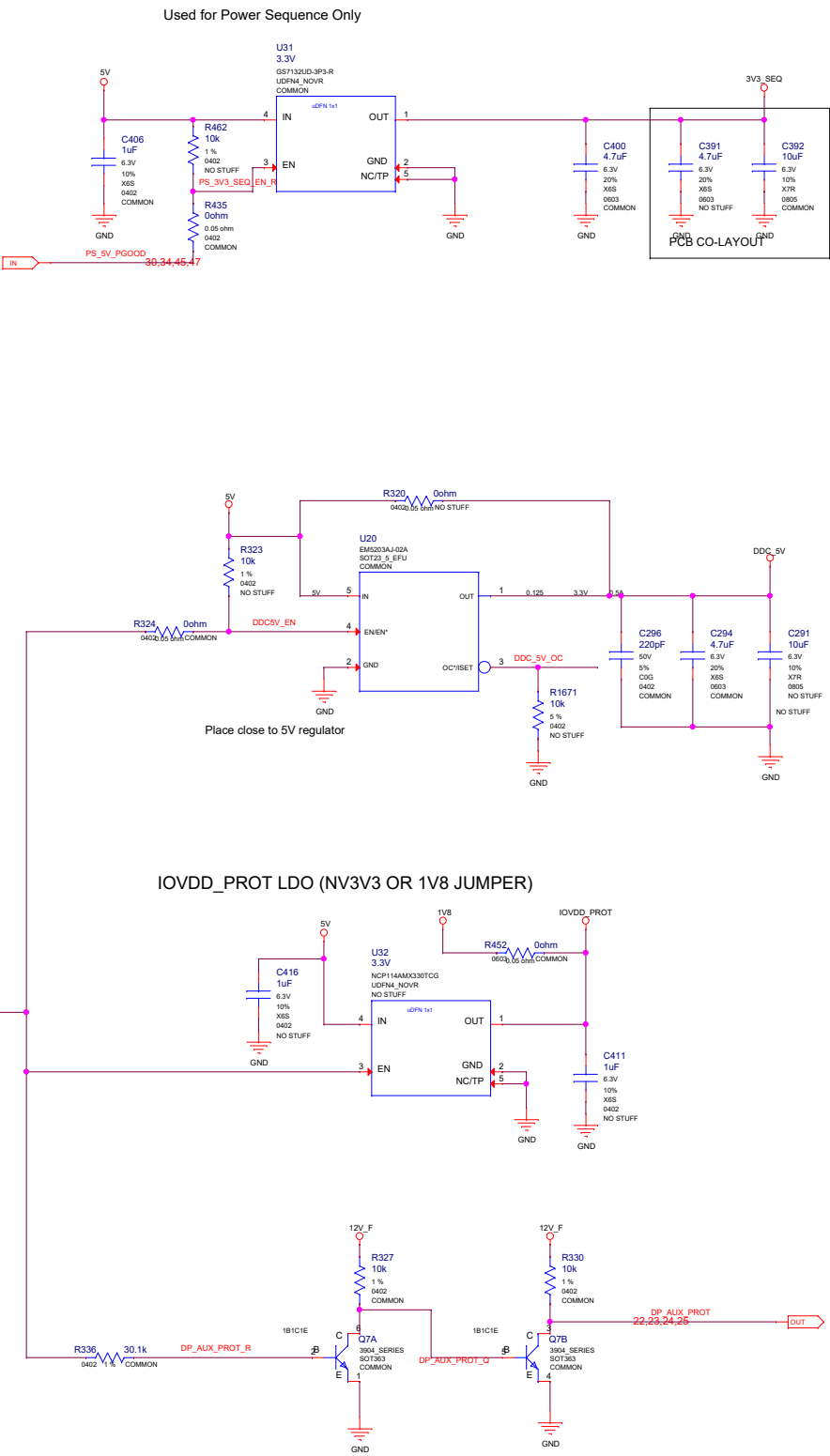


3V3\_SEQ

DDC\_5V

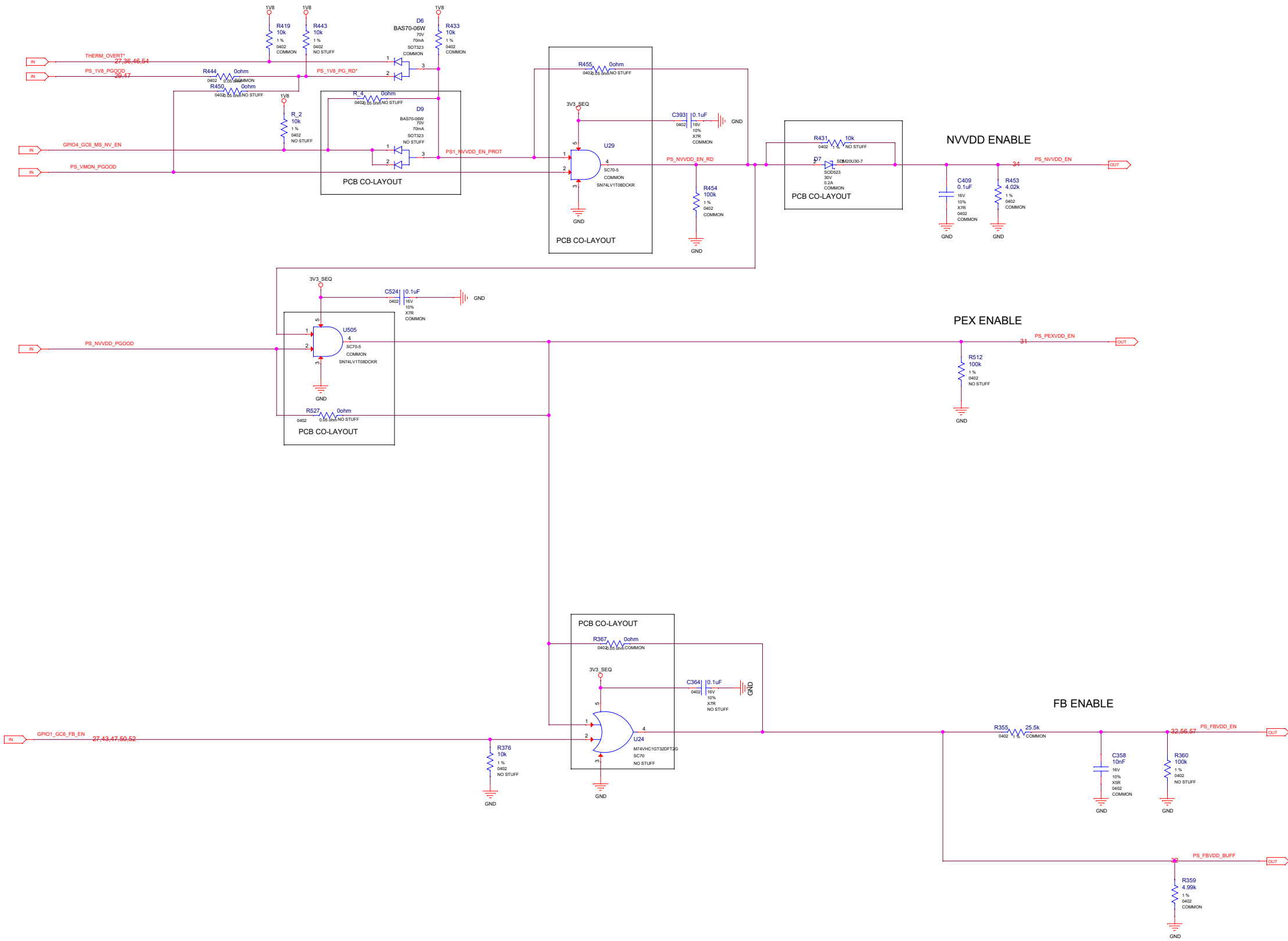
IOVDD\_PROT

DP\_AUX PROTECTION



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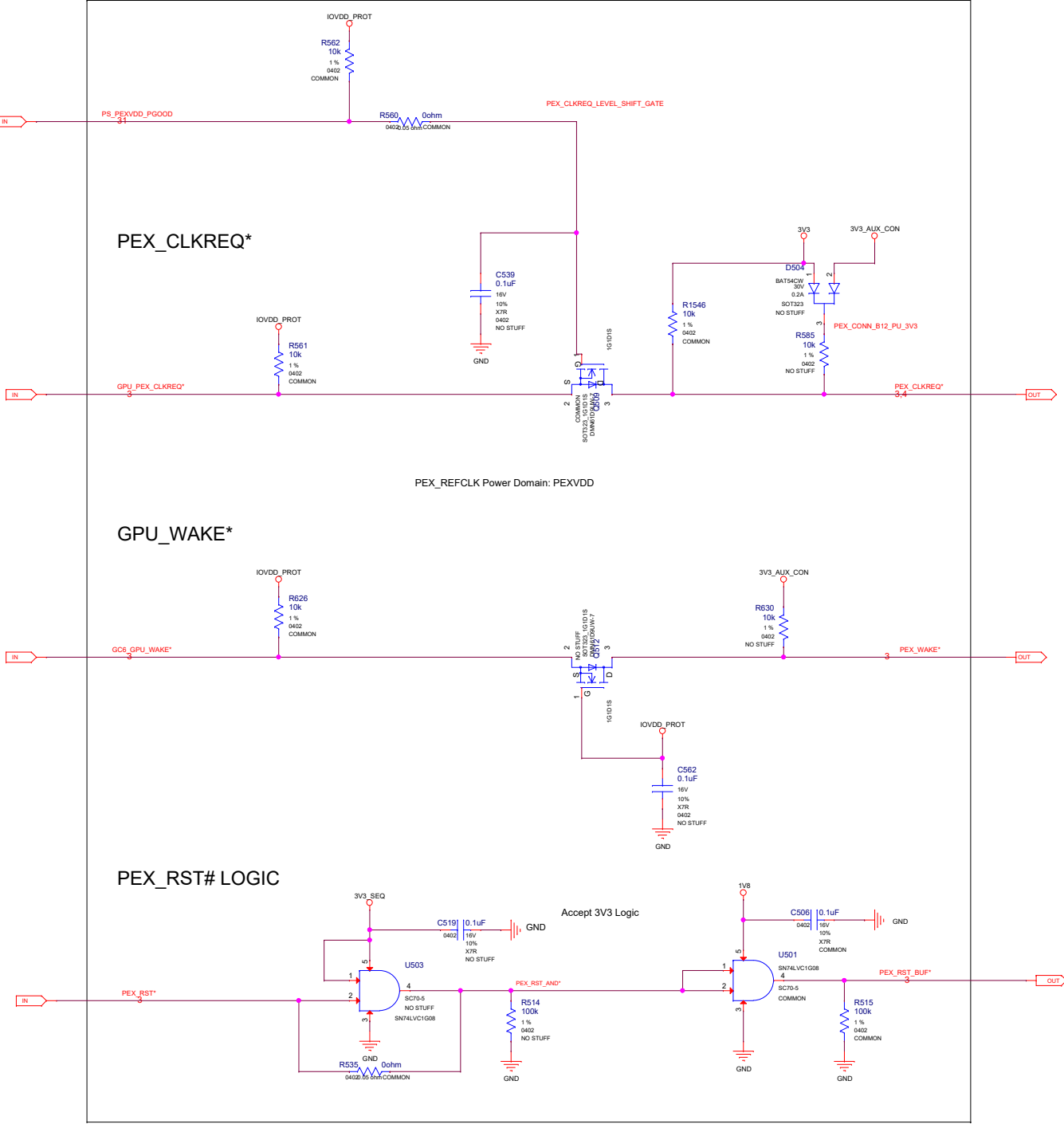


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ASSEMBLY  
PAGE DETAIL

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SEQ: NVVDD, PEX, FBVDDQ ENABLE


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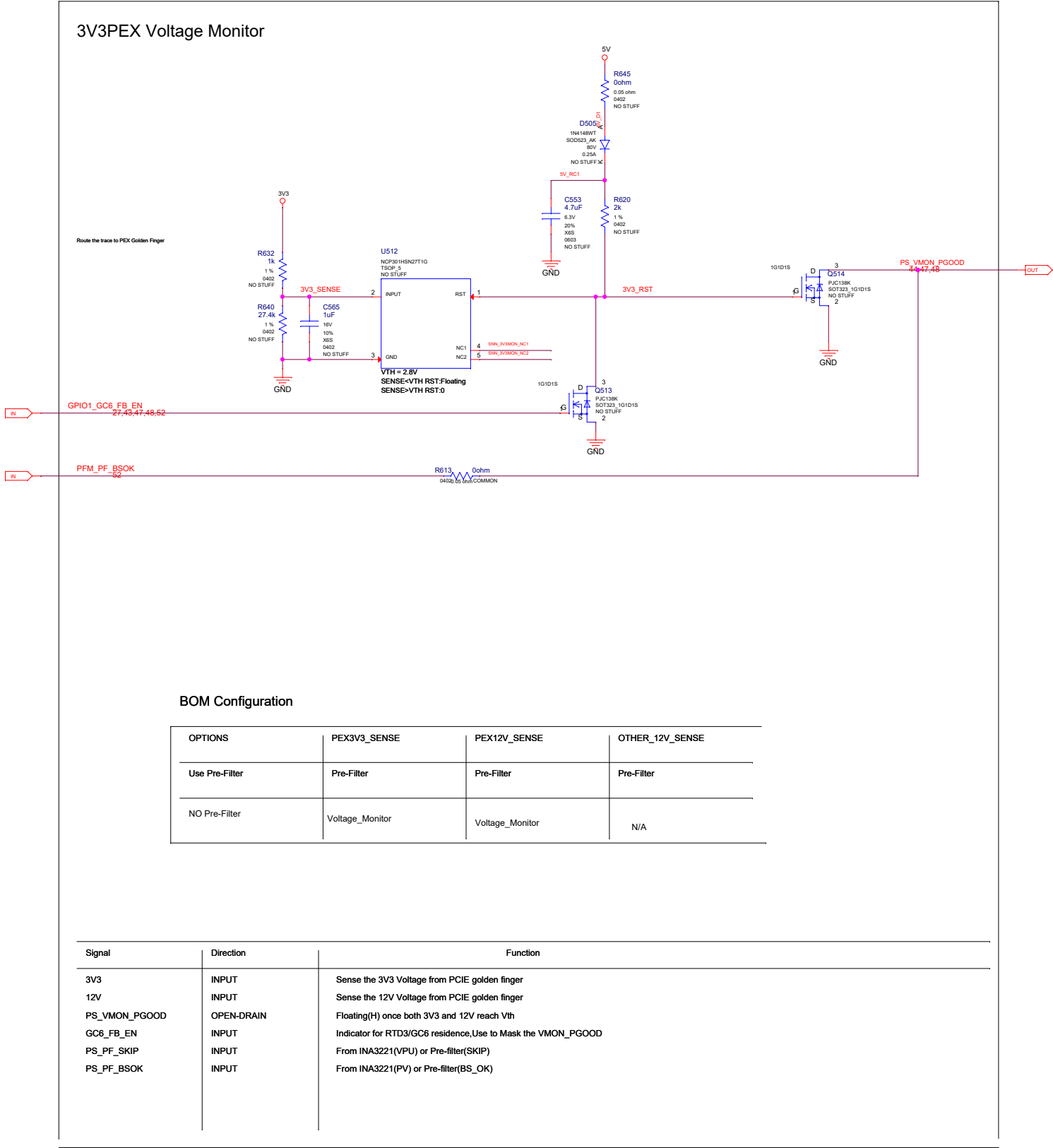


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ASSEMBLY  
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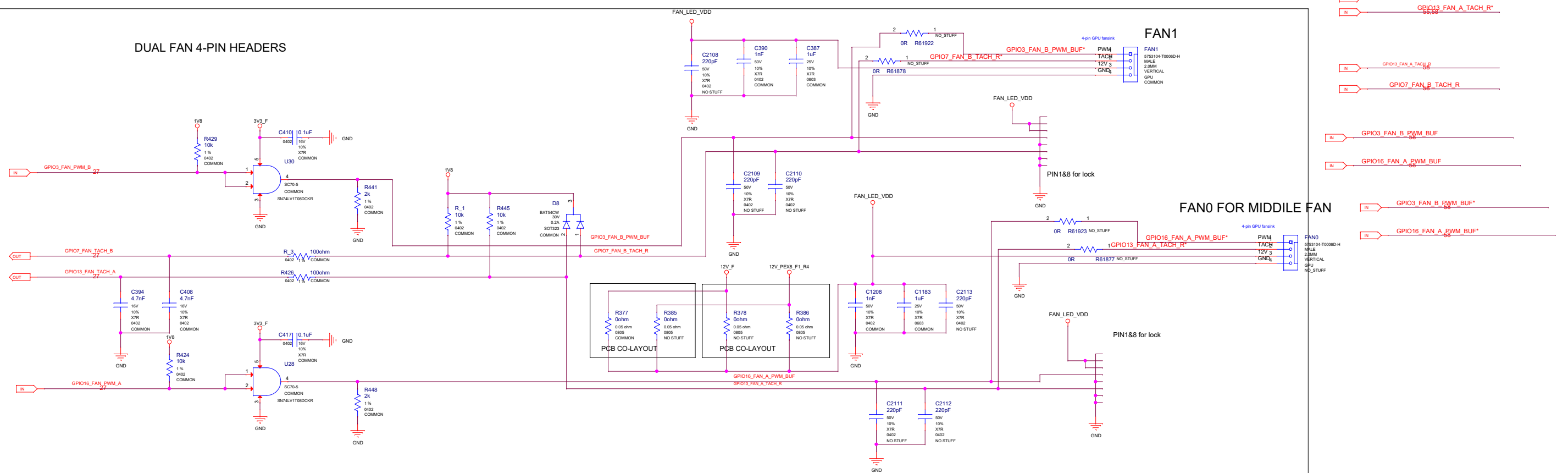
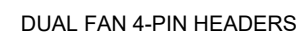
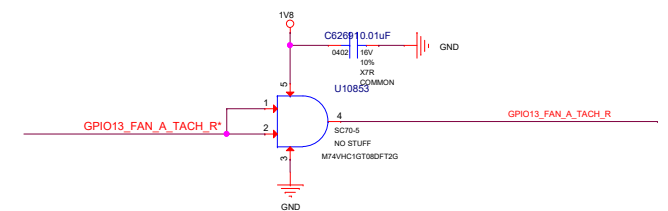
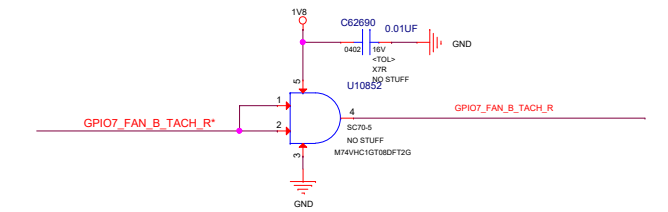
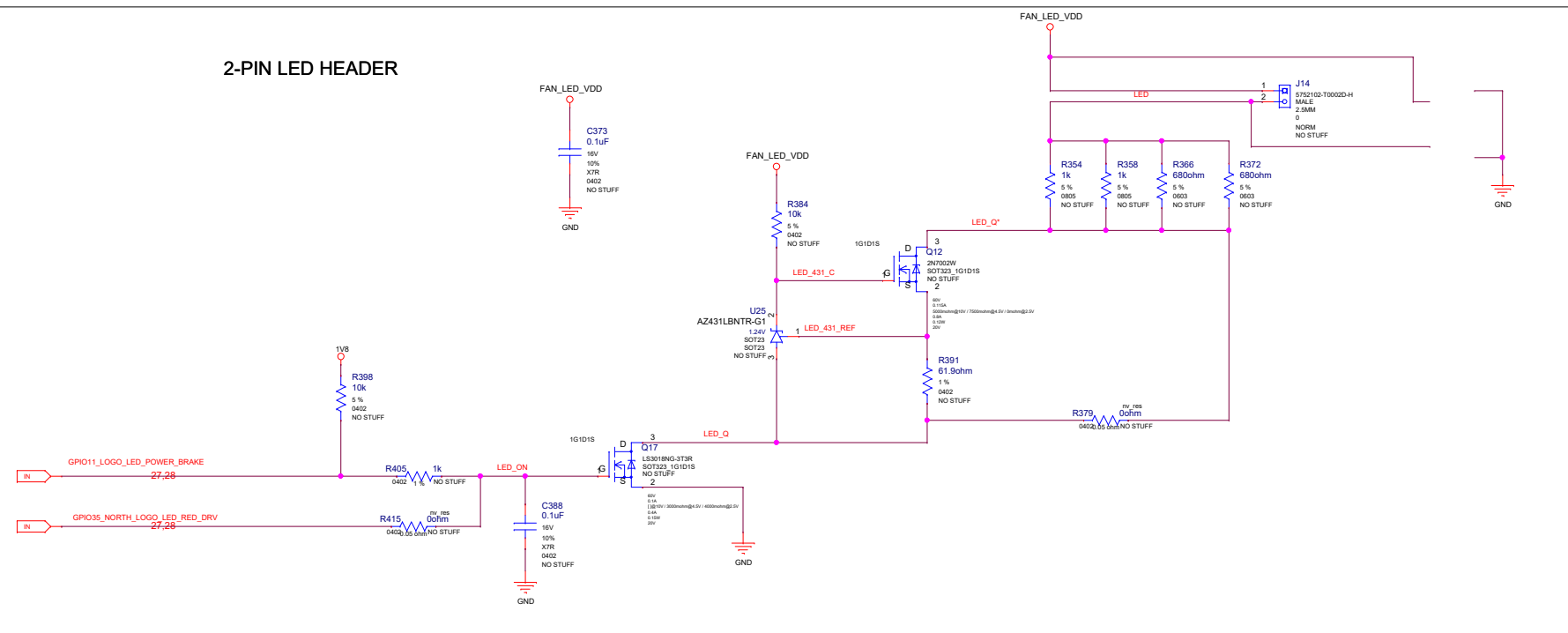
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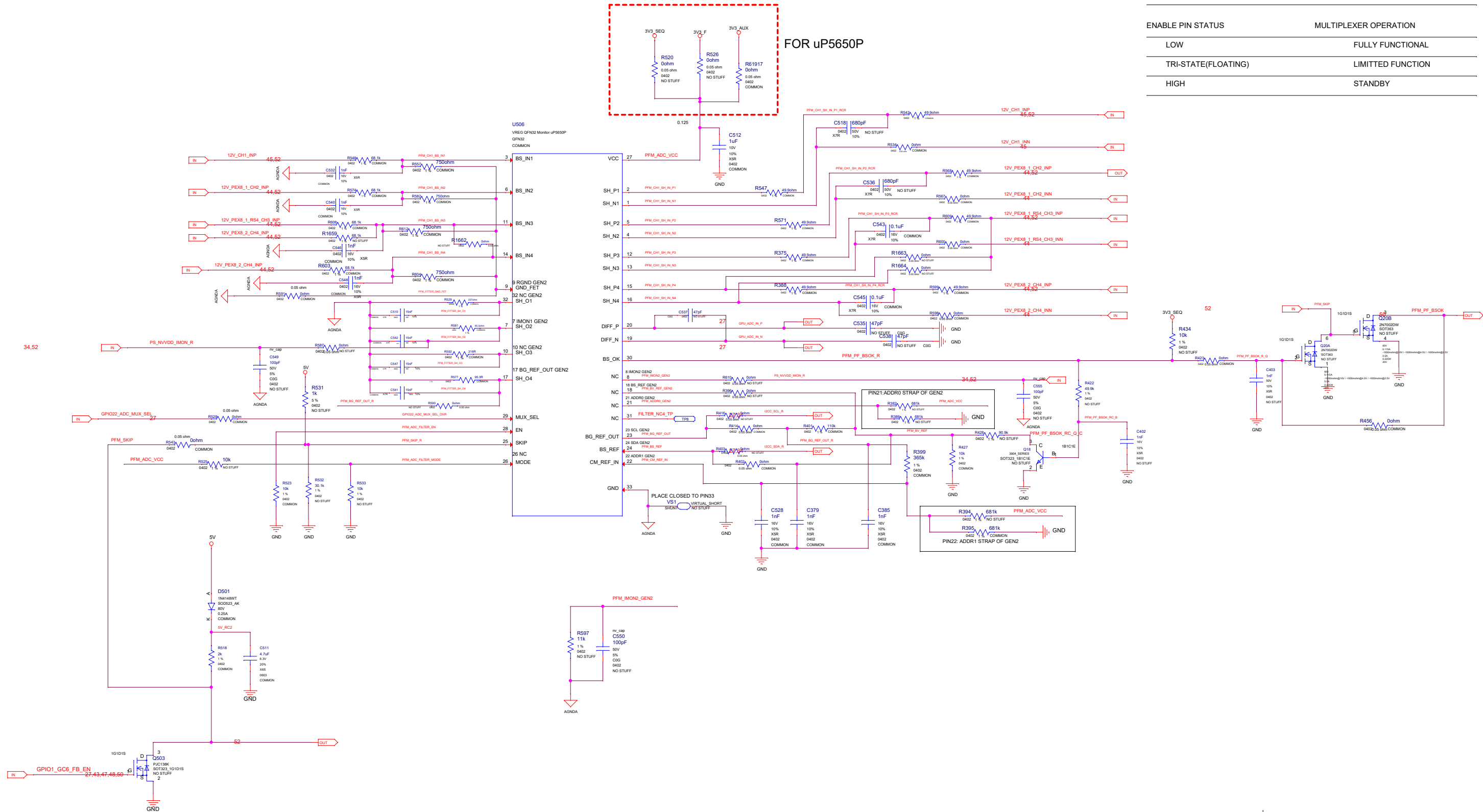
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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

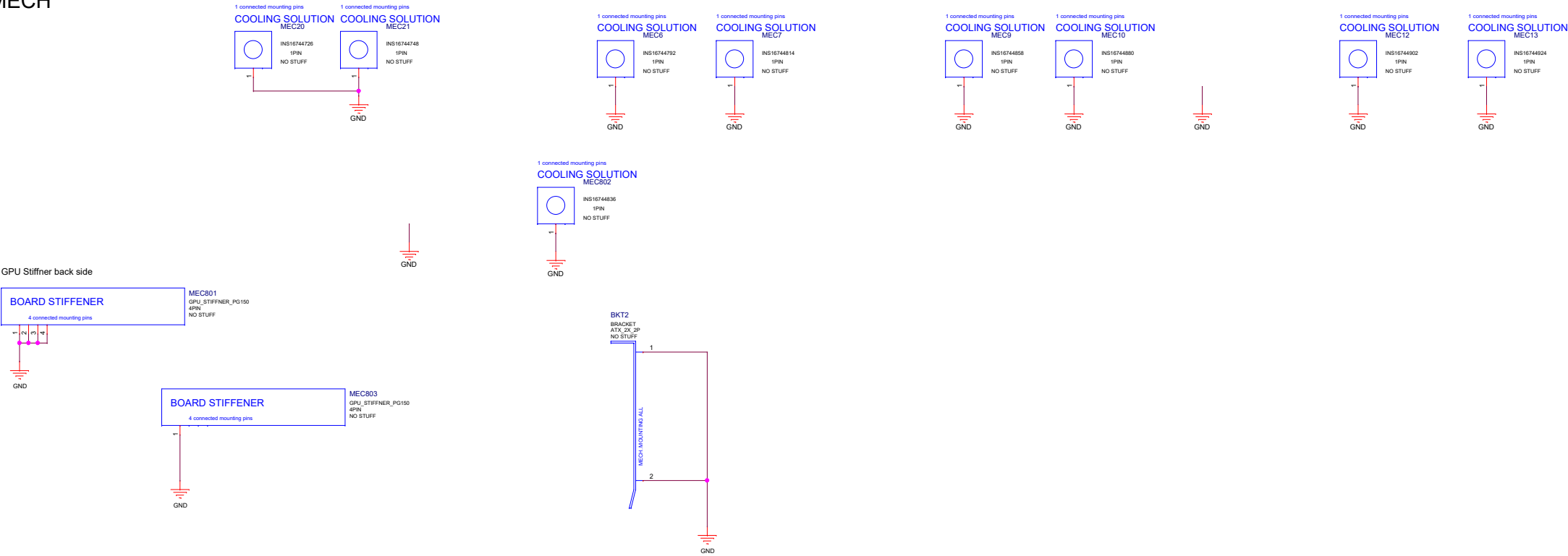
  

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY


ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

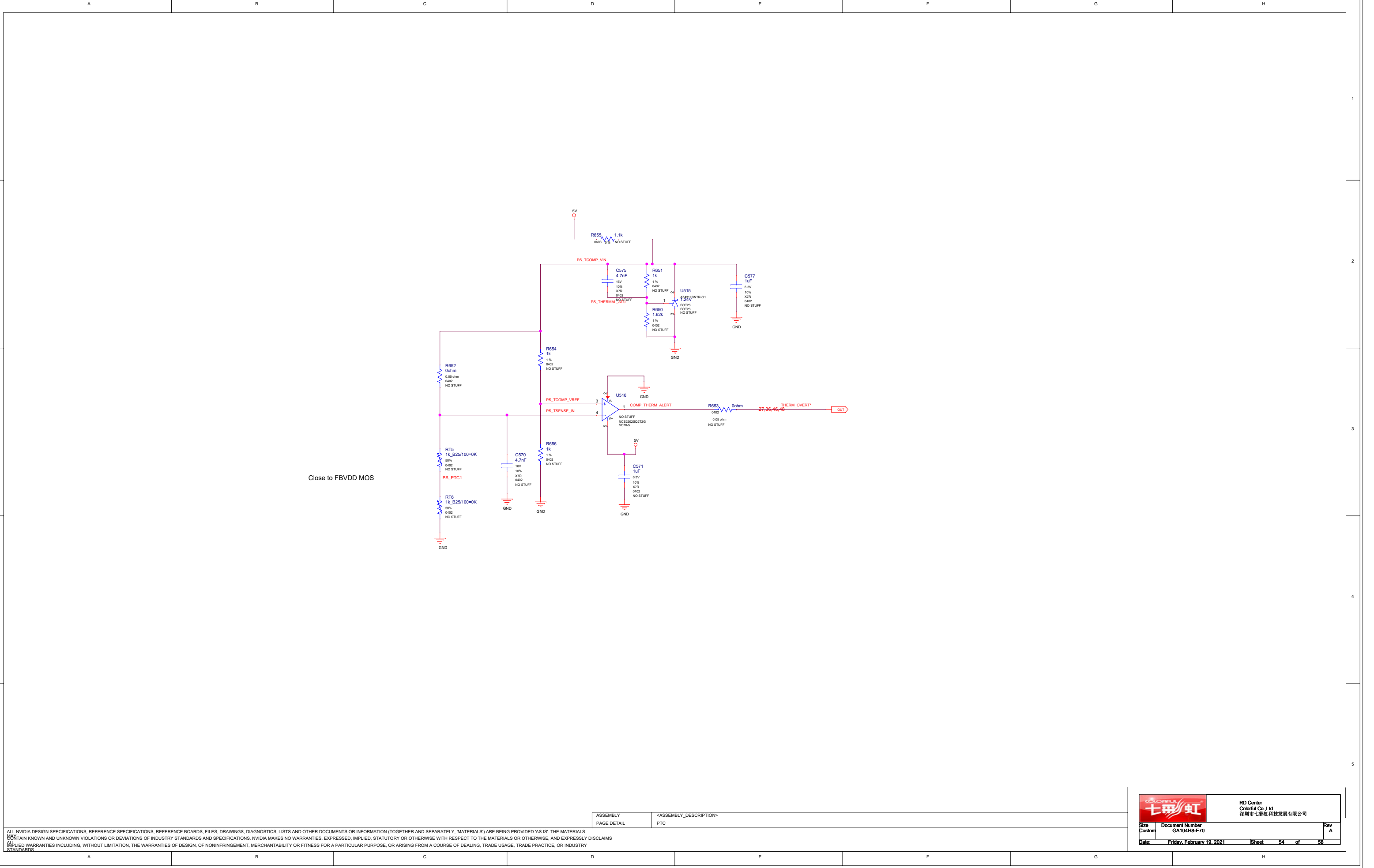
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NCP81273 EN VIH >1.5V, VIL < 0.7V  
UP9509/10 EN VIH >1.2V, VIL < 0.6V  
RT8817A EN VIH >1.2V, VIL < 0.6V

